MT6357 PMIC Datasheet

Version: 1.0
Release date: 2017-08-09

Specifications are subject to change without notice.

© 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Document Revision History

Revision	Date	Author	Description
1.0	2017-08-09	Zax Lo	First release

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table of Contents

Document Revision History **2**
Table of Contents **3**
1 Overview **5**
1.1 Features 5
1.2 Applications 5
1.3 General Descriptions 5
1.4 Ordering Information 6
1.5 Top Marking Definition 6
1.6 Pin Assignments and Descriptions 7
2 Electrical Characteristics **12**
2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range 12
2.2 Thermal Characteristic 13
2.3 Pin Voltage Range 14
2.4 Recommended Operating Range 18
2.5 Electrical Characteristics 19
2.6 Regulator Output 20
2.7 Driver 26
2.8 Audio CODEC 27
2.9 Battery Charger 32
2.10 BC1.2 33
2.11 Down Load Without Battery 34
2.12 AUXADC 35
2.13 Fuel Gauge 36
2.14 DCXO 37
3 Functional Descriptions **38**
3.1 General Descriptions 38
3.2 PMIC Functional Blocks 39
3.3 Register Table and Descriptions 59
4 Application Notes **251**
5 MT6357 Packaging **252**
5.1 Package Dimensions 252
Appendix **253**

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Lists of Figures and Tables

Figure 1-1. MT6357 VFBGA 209 (7.0x6.6mm) pin assignment (top view) 7
Figure 2-1. Audio Path THD+N vs. frequency 29
Figure 2-2. Audio path Xtalk vs. frequency @P_{OUT}=10mW 29
Figure 3-1. MT6357 block diagram 38
Figure 3-2. Power-on/off control sequence without XTAL by charger plug in or by pressing PWRKEY 40
Figure 3-3. Configuration for indicator LED drivers 43
Figure 3-4. LED drivers breath mode 43
Figure 3-5. Audio CODEC block diagram 46
Figure 3-6. Block diagram of battery charger 47
Figure 3-7. Flow chart of charging states 48
Figure 3-8. Fuel gauge block diagram and external connection 51
Figure 5-1. Package dimension 252

Table 1-1. MT6357 pin descriptions 7
Table 2-1. Absolute maximum ratings 12
Table 2-2. Pin voltage range 14
Table 2-3. Operation condition 18
Table 2-4. General electrical specifications 19
Table 2-5. Buck specifications 20
Table 2-6. LDO specifications 23
Table 2-7. Driver specifications 26
Table 2-8. Audio downlink specifications 27
Table 2-9. Audio uplink specifications 29
Table 2-10. MICBIAS specifications 31
Table 2-11. ACCDET specifications 31
Table 2-12. Charger specifications 32
Table 2-13. BC1.2 specifications 33
Table 2-14. Download without battery specifications 34
Table 2-15. AUXADC specifications 35
Table 2-16. Fuel gauge specifications 36
Table 2-17. XO specification 37
Table 2-18. Reference input buffer specification (XTAL1, buffer mode) 37
Table 3-1. Buck converter brief specifications 42
Table 3-2. LDO types and brief specifications 42
Table 3-3. Application and input range of ADC channels 50

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.6V ~ 5V
- 5 buck converters and 29 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- SPI interface
- USB Battery Charging Specification version BC1.2 Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 209-pin VFBGA package

1.2 Applications

MT6357 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6357 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 5 buck converters and 29 LDOs optimized for specific 2G/3G/4G smart phone subsystems.
Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6357 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6357 adopts SPI interface and two SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6357 is available in a 209-pin VFBGA package. The operating temperature ranges from -30 to +85°C.

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6357V/A		-30 ~ +85°C	VFBGA 209L

1.5 Top Marking Definition

MT6357V/A

$: random code
YYWW: Date code

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1.6 Pin Assignments and Descriptions

209	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VPA	VSYS_VPA	VSYS_VPA	VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	VCORE	VCORE		GND_VMODEM	VSYS_VMODEM	VSYS_VS1	GND_VS1	VS1	VCAMIO	A
B	GND_SMPS	VSYS_SMPS	GND_VPA	VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	GND_VCORE	VCORE	VMODEM	GND_VMODEM	VSYS_VMODEM	VSYS_VS1	GND_VS1	VS1	VIO18	B
C		VPROC_FB		VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	GND_VCORE	VCORE	VMODEM	GND_VMODEM					VS1_LDO1	C
D	AU_V18N	GND_VPROC_FB	VCORE_FB			D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	GND_VMODEM_FB		VRF18		D
E		FLYN	GND_VCORE_FB	VPA_FB		D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	VMODEM_FB	VS1_FB	VCN18	VRF12	VCAMD	E
F	FLYP	AVSS18_AUD	AU_LOLN	AU_LOLP	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND		VS2_LDO1		VS2_LDO2	F
G		AVDD18_AUD	AU_HPR		AU_HSN	AU_HSP	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND		VSYS_LDO1	VSRAM_PROC	VSRAM_OTHERS		G
H			AU_REFN		AVSS28_AUD	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND			VEFUSE	VCAMA	VDRAM	H
J	HP_EINT	AU_HPL		AU_VIN2_P	AU_VIN2_N	D_GND	D_GND	D_GND	D_GND	DVSS18_IO	D_GND			VUSB			VSIM1	J
K	AVDD28_AUD		AU_VIN0_P	AU_VIN0_N	AU_VIN1_P		VSYS_LDO3			DVDD18_IO		D_GND	VCN28		VIO28	VSIM2		K
L			AU_MICBIAS0		AU_VIN1_N		VAUD28			DVDD18_DIG		ISINK1		VFE28	VMC	VLDO28	VEMC	L
M	XTAL1	AVSS22_XO	AU_MICBIAS1	ACCDET	EXT_PMIC_EN1	EXT_PMIC_PG	SPI_MOSI	SPI_CLK	SPI_MISO	CHG_DM	CHG_DP		BATSNS	AUD_SYNC_MOSI		VIBR		M
N	XTAL2	AVSS22_XO_ISO	UVLO_VTH	FCHR_ENB	EXT_PMIC_EN2		SRCLKEN_IN0	SRCLKEN_IN1	VSYSSNS			PCHR_LED	ISENSE	AUD_DAT_MOSI1		VMCH	VSYS_LDO2	N
P	AVSS22_XOBUF	AVSS22_XO_ISO	XO_WCN		PMU_TESTMODE		AVSS18_AUXADC		FSOURCE		RTC32K_2V8		VDRV	RTC32K_1V8_0	AUD_DAT_MOSI0	AUD_CLK_MOSI	VCN33	P
R	AVSS22_XOBUF	XO_NFC	XO_SOC	PWRKEY	RESETB		AVDD18_AUXADC	SPI_CSN	TREF	CS_N	CHRLDO	VRTC28	BATON		RTC32K_1V8_1	AUD_CLK_MISO	AUD_DAT_MISO1	R
T	XO_CEL	XO_EXT		VXO22	VAUX18		AUXADC_VIN	WDTRSTB_IN		CS_P	VCDT		GND_VREF	VREF		AUD_SYNC_MISO	AUD_DAT_MISO0	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 1-1. MT6357 VFBGA 209 (7.0x6.6mm) pin assignment (top view)

Table 1-1. MT6357 pin descriptions

Ball	Symbol	I/O	Description
A4, B4, C4	VSYS_VPROC	PWR	Power supply of VPROC
A6, A7, B6, B7, C6, C7	VPROC	O	SW node of VPROC
A5, B5, C5	GND_VPROC	GND	VPROC ground
C2	VPROC_FB	I	BUCK VPROC feedback pin
D2	GND_VPROC_FB	I	Remote sense on ground of VPROC
A8, B8, C8	VSYS_VCORE	PWR	Power supply of VCORE
A9, A10, B10, C10	VCORE	O	SW node of VCORE

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	I/O	Description
B9, C9	GND_VCORE	GND	VCORE ground
D3	VCORE_FB	I	BUCK VCORE feedback pin
E3	GND_VCORE_FB	I	Remote sense on ground of VCORE
A13, B13	VSYS_VMODEM	PWR	Power supply of VMODEM
B11, C11	VMODEM	O	SW node of VMODEM
A12, B12, C12	GND_VMODEM	GND	VMODEM ground
E13	VMODEM_FB	I	BUCK VMODEM feedback pin on Vout
D14	GND_VMODEM_FB	I	Remote sense on ground of VMODEM Vout
A14, B14	VSYS_VS1	PWR	Power supply of VS1
A16, B16	VS1	O	SW node of VS1
A15, B15	GND_VS1	GND	VS1 ground
E14	VS1_FB	I	BUCK VS1 feedback pin
A2, A3	VSYS_VPA	PWR	Power supply of VPA
A1	VPA	O	SW node of VPA
B3	GND_VPA	GND	VPA ground
E4	VPA_FB	I	BUCK VPA feedback pin on Vout
B2	VSYS_SMPS	PWR	Power supply of buck controller
B1	GND_SMPS	GND	GND of buck controller
L14	VFE28	O	VFE28 output voltage
K13	VCN28	O	VCN28 output voltage
H16	VCAMA	O	VCAMA output voltage
R9	TREF	O	TREF output voltage
T4	VXO22	O	VXO22 output voltage
L7	VAUD28	O	VAUD28 output voltage
T5	VAUX18	O	VAUX18 output voltage
P17	VCN33	O	VCN33 output voltage
J17	VSIM1	O	VSIM1 output voltage
K16	VSIM2	O	VSIM2 output voltage
L16	VLDO28	O	VLDO28 output voltage
K15	VIO28	O	VIO28 output voltage
L15	VMC	O	VMC output voltage
N16	VMCH	O	VMCH output voltage
L17	VEMC	O	VEMC33 output voltage
M16	VIBR	O	VIBR output voltage
J14	VUSB	O	VUSB output voltage
A17	VCAMIO	O	VCAMIO output voltage
E15	VCN18	O	VCN18 output voltage
D16	VRF18	O	VRF18 output voltage
B17	VIO18	O	VIO18 output voltage
H15	VEFUSE	O	VEFUSE output voltage
E17	VCAMD	O	VCAMD output voltage

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	I/O	Description
E16	VRF12	O	VRF12 output voltage
G15	VSRAM_PROC	O	VSRAM_PROC output voltage
G16	VSRAM_OTHERS	O	VSRAM_OTHERS output voltage
H17	VDRAM	O	VDRAM output voltage
C17	VS1_LDO1	PWR	2V power supply of SLDO1
F15	VS2_LDO1	PWR	Power supply of SLDO1
F17	VS2_LDO2	PWR	Power supply of SLDO2
G14	VSYS_LDO1	PWR	Power supply input of LDO group1
N17	VSYS_LDO2	PWR	Power supply input of LDO group2
K7	VSYS_LDO3	PWR	Power supply input of LDO group3
N4	FCHR_ENB	I	Force charging disable pin (merged with HOMEKEY, same as MT6351)
N13	ISENSE	I	Positive terminal for battery's charging current sensing resistor
M13	BATSNS	I	Negative terminal for battery's charging current sensing resistor
N9	VSYSSNS	I	VSYS supply input for internal block and UVLO detection
R13	BATON	I	Battery NTC pin for battery and its temperature sensing
T11	VCDT	I	Fractional charger input voltage for charger detection
P13	VDRV	O	Charger current drive output
R11	CHRLDO	O	CHRLDO output voltage
M10	CHG_DM	I	USB D- for BC1.2 standard
M11	CHG_DP	I	USB D+ for BC1.2 standard
N12	PCHR_LED	I	Pre-Charge Indicator
N3	UVLO_VTH	I	UVLO threshold control pin
T14	VREF	O	Bandgap reference voltage
T13	GND_VREF	GND	Ground for bandgap
P11	RTC32K_2V8	O	VRTC domain 32kHz clock output
R12	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
R4	PWRKEY	I	PWRKEY button
R5	RESETB	O	System reset release signal
P5	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
M5	EXT_PMIC_EN1	O	Ext chip enable pin1
N5	EXT_PMIC_EN2	O	Ext chip enable pin2
M6	EXT_PMIC_PG	I	Ext chip enable PGOOD Detect
R10	CS_N	I	Fuel gauge ADC input pin
T10	CS_P	I	Fuel gauge ADC input pin
R7	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
P7	AVSS18_AUXADC	GND	AUXADC ground
T7	AUXADC_VIN	I	AUXADC input

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	I/O	Description
P16	AUD_CLK_MOSI	I	Audio control interface
P15	AUD_DAT_MOSI0	I/O	Audio control interface
N14	AUD_DAT_MOSI1	I/O	Audio control interface
M14	AUD_SYNC_MOSI	I/O	Audio control interface
R16	AUD_CLK_MISO	O	Audio control interface
T17	AUD_DAT_MISO0	I/O	Audio control interface
R17	AUD_DAT_MISO1	I/O	Audio control interface
T16	AUD_SYNC_MISO	I/O	Audio control interface
M8	SPI_CLK	I	SPI control interface
R8	SPI_CSN	I/O	SPI control interface
M9	SPI_MISO	I/O	SPI control interface
M7	SPI_MOSI	I/O	SPI control interface
T8	WDTRSTB_IN	I	Watchdog reset from AP
N7	SRCLKEN_IN0	I	Source clock enable pin 0
N8	SRCLKEN_IN1	I	Source clock enable pin 1
L10	DVDD18_DIG	PWR	VDIG18 output voltage
K10	DVDD18_IO	PWR	Digital IO power
J10	DVSS18_IO	GND	Digital IO power GND
P14	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
R15	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
P9	FSOURCE	PWR	EFUSE power source
G3	AU_HPR	O	Earphone right channel output
J2	AU_HPL	O	Earphone left channel output
H3	AU_REFN	GND	Audio reference ground
G5	AU_HSN	O	Handset negative output
G6	AU_HSP	O	Handset positive output
F4	AU_LOLP	O	Lineout positive output
F3	AU_LOLN	O	Lineout negative output
M4	ACCDET	I	Accessory detection input
L3	AU_MICBIAS0	O	Microphone Bias 0
M3	AU_MICBIAS1	O	Microphone Bias 1
K3	AU_VIN0_P	I	Microphone channel 0 positive input
K4	AU_VIN0_N	I	Microphone channel 0 negative input
K5	AU_VIN1_P	I	Microphone channel 1 positive input
L5	AU_VIN1_N	I	Microphone channel 1 negative input
J4	AU_VIN2_P	I	Microphone channel 2 positive input
J5	AU_VIN2_N	I	Microphone channel 2 negative input
J1	HP_EINT	I	HPL detection
G2	AVDD18_AUD	PWR	1.8V power supply of audio
F2	AVSS18_AUD	GND	Audio DL ground

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	I/O	Description
F1	FLYP	O	Flying capacitor top
E2	FLYN	O	Flying capacitor bottom
D1	AU_V18N	PWR	Audio -1.8V supply
K1	AVDD28_AUD	PWR	Power supply of Audio UL
H5	AVSS28_AUD	GND	Audio UL ground
L12	ISINK1	I	ISINK channel 1
P1, R1	AVSS22_XOBUF	GND	Ground for XO
P3	XO_WCN	O	26MHz output to Conn. RF
T1	XO_CEL	O	26MHz output to Cell. RF
R2	XO_NFC	O	26MHz output to NFC
R3	XO_SOC	O	26MHz output to SOC
T2	XO_EXT	O	26MHz output to UFS
M2	AVSS22_XO	GND	Ground for XO
M1	XTAL1	I/O	XTAL input 1
N1	XTAL2	I/O	XTAL input 2
N2, P2	AVSS22_XO_ISO	GND	Connect to GSUB for DCXO noise isolation
D6, D7, D8, D9, D10, D11, D12, D13, E6, E7, E8, E9, E10, E11, E12, F5, F6, F7, F8, F9, F10, F11, F12, F13, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J11, K12	D_GND	GND	Ground

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range(1)	Steady state	-0.5		6	V
	Transient (< 10 ms)	-0.5		7	V
Non-Battery Power Pin(2)	Steady state	-0.5		5	V
Signal Pins(3)	Steady state	-0.5		Vxx+0.5(3)	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

Note:

1. VSYS_XXX/Vxxx(BUCK SW Node)/BATSNS/ISENSE/VSYSSNS→Battery Input Pin
2. Non-Battery Power Pin→Reference Table1-1(PWR Pin but not connected with Battery)
3. Vxx=Maximum Operating Voltage(Refer to Table2-2)

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		51.8		°C/W

Note: The device is mounted on an 8-metal-layer PCB and modeled per JEDEC51-9 condition.

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6357 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A4, B4, C4	VSYS_VPROC	0~5.0	v
A6, A7, B6, B7, C6, C7	VPROC	0~5.0	v
A5, B5, C5	GND_VPROC	0	v
C2	VPROC_FB	0~5.0	v
D2	GND_VPROC_FB	0	v
A8, B8, C8	VSYS_VCORE	0~5.0	v
A9, A10, B10, C10	VCORE	0~5.0	v
B9, C9	GND_VCORE	0	v
D3	VCORE_FB	0~5.0	v
E3	GND_VCORE_FB	0	v
A13, B13	VSYS_VMODEM	0~5.0	v
B11, C11	VMODEM	0~5.0	v
A12, B12, C12	GND_VMODEM	0	v
E13	VMODEM_FB	0~5.0	v
D14	GND_VMODEM_FB	0	v
A14, B14	VSYS_VS1	0~5.0	v
A16, B16	VS1	0~5.0	v
A15, B15	GND_VS1	0	v
E14	VS1_FB	0~5.0	v
A2, A3	VSYS_VPA	0~5.0	v
A1	VPA	0~5.0	v
B3	GND_VPA	0	v
E4	VPA_FB	0~5.0	v
B2	VSYS_SMPS	0~5.0	v
B1	GND_SMPS	0	v
L14	VFE28	0~5.0	v
K13	VCN28	0~5.0	v
H16	VCAMA	0~5.0	v
R9	TREF	0~1.98	v
T4	VXO22	0~2.42	v
L7	VAUD28	0~5.0	v
T5	VAUX18	0~5.0	v
P17	VCN33	0~5.0	v
J17	VSIM1	0~5.0	v
K16	VSIM2	0~5.0	v
L16	VLDO28	0~5.0	v
K15	VIO28	0~5.0	v
L15	VMC	0~5.0	v
N16	VMCH	0~5.0	v
L17	VEMC	0~5.0	v

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	Voltage range	Unit
M16	VIBR	0~5.0	v
J14	VUSB	0~3.63	v
A17	VCAMIO	0~2.2	v
E15	VCN18	0~2.2	v
D16	VRF18	0~2.2	v
B17	VIO18	0~2.2	v
H15	VEFUSE	0~2.2	v
E17	VCAMD	0~2.2	v
E16	VRF12	0~2.2	v
G15	VSRAM_PROC	0~1.4	v
G16	VSRAM_OTHERS	0~1.4	v
H17	VDRAM	0~2.2	v
C17	VS1_LDO1	0~2.2	v
F15	VS2_LDO1	0~2.2	v
F17	VS2_LDO2	0~2.2	v
G14	VSYS_LDO1	0~5.0	v
N17	VSYS_LDO2	0~5.0	v
K7	VSYS_LDO3	0~5.0	v
N4	FCHR_ENB	0~5.0	v
N13	ISENSE	0~5.0	v
M13	BATSNS	0~5.0	v
N9	VSYSSNS	0~5.0	v
R13	BATON	0~2.8	v
T11	VCDT	0~2.94	v
P13	VDRV	0~5.0	v
R11	CHRLDO	0~2.94	v
M10	CHG_DM	0~3.3	v
M11	CHG_DP	0~3.3	v
N12	PCHR_LED	0~5.0	v
N3	UVLO_VTH	0~3.3	v
T14	VREF	0~1.32	v
T13	GND_VREF	0	v
P11	RTC32K_2V8	0~2.98	v
R12	VRTC28	0~2.98	v
R4	PWRKEY	0~5.0	v
R5	RESETB	0~1.98	v
P5	PMU_TESTMODE	0~5.0	v
M5	EXT_PMIC_EN1	0~5.0	v
N5	EXT_PMIC_EN2	0~5.0	v
M6	EXT_PMIC_PG	0~5.0	v
R10	CS_N	-0.1~0.1	v
T10	CS_P	-0.1~0.1	v
R7	AVDD18_AUXADC	0~1.9	v
P7	AVSS18_AUXADC	0	v
T7	AUXADC_VIN	0~1.9	v
P16	AUD_CLK_MOSI	0~1.98	v

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	Voltage range	Unit
P15	AUD_DAT_MOSI0	0~1.98	v
N14	AUD_DAT_MOSI1	0~1.98	v
M14	AUD_SYNC_MOSI	0~1.98	v
R16	AUD_CLK_MISO	0~1.98	v
T17	AUD_DAT_MISO0	0~1.98	v
R17	AUD_DAT_MISO1	0~1.98	v
T16	AUD_SYNC_MISO	0~1.98	v
M8	SPI_CLK	0~1.98	v
R8	SPI_CSN	0~1.98	v
M9	SPI_MISO	0~1.98	v
M7	SPI_MOSI	0~1.98	v
T8	WDTRSTB_IN	0~1.98	v
N7	SRCLKEN_IN0	0~1.98	v
N8	SRCLKEN_IN1	0~1.98	v
L10	DVDD18_DIG	0~1.98	v
K10	DVDD18_IO	0~1.98	v
J10	DVSS18_IO	0	v
P14	RTC32K_1V8_0	0~1.98	v
R15	RTC32K_1V8_1	0~1.98	v
P9	FSOURCE	0~1.98	v
G3	AU_HPR	-1.98~1.98	v
J2	AU_HPL	-1.98~1.98	v
H3	AU_REFN	0	v
G5	AU_HSN	-1.98~1.98	v
G6	AU_HSP	-1.98~1.98	v
F4	AU_LOLP	-1.98~1.98	v
F3	AU_LOLN	-1.98~1.98	v
M4	ACCDET	0 ~ 2.94	v
L3	AU_MICBIAS0	0 ~ 2.94	v
M3	AU_MICBIAS1	0 ~ 2.94	v
K3	AU_VIN0_P	0 ~ 2.94	v
K4	AU_VIN0_N	0 ~ 2.94	v
K5	AU_VIN1_P	0 ~ 2.94	v
L5	AU_VIN1_N	0 ~ 2.94	v
J4	AU_VIN2_P	0 ~ 2.94	v
J5	AU_VIN2_N	0 ~ 2.94	v
J1	HP_EINT	0 ~ 2.94	v
G2	AVDD18_AUD	0~1.98	v
F2	AVSS18_AUD	0	v
F1	FLYP	0~1.98	v
E2	FLYN	-1.98~0	v
D1	AU_V18N	-1.98~0	v
K1	AVDD28_AUD	0~2.94	v
H5	AVSS28_AUD	0	v
L12	ISINK1	0~5.0	v
P1, R1	AVSS22_XOBUF	0	v

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Ball	Symbol	Voltage range	Unit
P3	XO_WCN	0~1.98	v
T1	XO_CEL	0~1.98	v
R2	XO_NFC	0~1.21	v
R3	XO_SOC	0~1.21	v
T2	XO_EXT	0~1.21	v
M2	AVSS22_XO	0	v
M1	XTAL1	-0.2~2.2	v
N1	XTAL2	0.2~1.7	v
N2, P2	AVSS22_XO_ISO	0	v
D6, D7, D8, D9, D10, D11, D12, D13, E6, E7, E8, E9, E10, E11, E12, F5, F6, F7, F8, F9, F10, F11, F12, F13, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J11, K12	D_GND	0	v

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Ambient temperature (TA)		-30		85	°C
Junction temperature (TJ)		-30		125	°C
Operating input voltage		3.15 (note)		5	V

Note: This minimum input voltage still needs to check the detailed test conditions for each function in specification table.

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.5 Electrical Characteristics

VBAT = 2.6V ~ 5V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Standby without 32K XTAL	Low-power mode		560	640	μA
Power down leakage current without 32K XTAL	VBAT=4.5V, Temp=25°C			80	uA
Under Voltage (UV)					
Under voltage falling threshold		2.55	2.6	2.65	V
Under voltage rising threshold (UVLO_VTHH) w/o charger	R=200K	2.95	3.0	3.05	V
Under voltage rising threshold (UVLO_VTHH) w/i charger	R=200K	2.75	2.8	2.85	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY/FCHR_ENB					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time			32		ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.7*VIO			V
Control input low (SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		°C
Shut-down release threshold			110		°C

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VPROC					
Turn-on overshoot	Vout=1.15V No load			10	%
OCP(Over Current Protect)		Imax*1.2		7.5	A
Efficiency	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=100mA		86		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=500mA		87		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=1.0A		87		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=5A		67		%
Soft start	Vout=1.15V No load			200	us
Switching Frequency	VBAT=3.8V, Iout=0.8A	1.87	2.2	2.53	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp
Load transient	VBAT=3.8V/Vout=1.15V I_Load = 0.02A to 1.2A (Tr/Tf=1us)	-5.55		5.55	%
Line transient	Vbat=3.8V to 4.5V, Vo=1.15V I_Load= 0.5*Imax (Tr/Tf=15us)	-5.55		5.55	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.15V to 5.0V I_Load= PWM Load	-5.5		5.5	mV
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.15V to 5.0V I_Load= PFM Load	-5.5		20	mV
Output Discharge Switch On Resistance				50	Ω
Buck – VCORE					
Turn-on overshoot	Vout=1.15V No load			10	%
OCP(Over Current Protect)		Imax*1.2		7.5	A
Efficiency	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=100mA		85		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=500mA		86		%
	VBAT=4.0V, Vout=1.15V,		87		%

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR.Max=30mΩ I_Load=1.0A				
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=5A		67		%
Soft start	Vout=1.15V No load			200	us
Switching Frequency	VBAT=3.8V, Iout=0.8A	1.87	2.2	2.53	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp
Load transient	VBAT=3.8V/Vout=1.15V I_Load=0.03A to 1.4A (Tr/Tf=2us)	-5.55		5.55	%
Line transient	Vbat=3.8V to 4.5V, Vo=1.15V I_Load= 0.5*Imax (Tr/Tf = 15us)	-5.55		5.55	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.15V to 5.0V I_Load=PWM Load	-5.5		5.5	mV
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.15V to 5.0V I_Load=PFM Load	-5.5		20	mV
Output Discharge Switch On Resistance				50	Ω
Buck – VMODEM					
Turn-on overshoot	Vout=1.15V No load			10	%
OCP(Over Current Protect)		Imax*1.2		4	A
Efficiency	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=30mA		86		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=100mA		86		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=400mA		87		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=1560mA		79		%
	VBAT=4.0V, Vout=1.15V, L_DCR.Max=30mΩ I_Load=2000mA		76		%
Soft start	Vout=1.15V No load			1500	us
Switching Frequency	VBAT=3.8V, Iout=0.8A	1.87	2.2	2.53	MHz
Output ripple voltage (PWM)	VBAT=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Conditions	Min.	Typical	Max.	Unit
Load transient	VBAT=3.8V,Vo=1.15V I_Load=50 mA to 700 mA (Tr/Tf=1us)	-4.15		4.9	%
Line transient	VBAT=3.8V to 4.5V,Vo=1.15V I_Load= 1A (Tr/Tf = 15us)	-4.15		4.9	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.15V to 5.0V I_Load=PWM Load	-1		1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.15V to 5.0V I_Load= PFM Load	-1		3.6	%
Output Discharge Switch On Resistance				120	Ω
Buck – VPA					
Turn-on overshoot	Vo =3.4V , No load			10	%
OCP(Over Current Protect)	Vo =3.4V		3.2		A
Efficiency	VBAT=4V, Vout=0.5V, L_DCR.Max=53mΩ I_Load=40mA		75		%
	VBAT=4V, Vout=1.2V, L_DCR.Max=53mΩ I_Load=200mA		83		%
	VBAT=4V, Vout=2.4V, L_DCR.Max=53mΩ I_Load=400mA		90		%
	VBAT=4V, Vout=3.4V, L_DCR.Max=53mΩ I_Load=650mA		93		%
	VBAT=4V, Vout=3.4V, L_DCR.Max=53mΩ I_Load=800mA		92		%
Soft start	VBAT=3.8 No load Vo=0.5V		250		us
Switching Frequency	PWM Mode , Vout=3.4V	1.8	2	2.2	MHz
Output ripple voltage	a. PFM ripple b. PWM ripple c. PWM ripple @ 0.2V < VBAT-VPA < 1.0V 20MHz measurement BW			a. 150 b. 50 c. 100	mVp-p
Load transient	VBAT=4.5V, Vout=3.4V ILOAD= 50mA <-> 800mA (Tr/Tf=1.6us)			400	mV
Line transient	Vbat=3.8V to 4.5V Vo=1.7V I_Load= 0.2A (Tr/Tf = 15us)			200	mV
DC accuracy (Included Line/Load regulation)	VBAT=3.15V to 5.0V Vout=0.5~1V I_load=PWM Load	-20		40	mV

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Conditions	Min.	Typical	Max.	Unit
DC accuracy (Included Line/Load regulation)	VBAT=3.15V to 5.0V VBAT– Vout ≥ 600 mV Vout ≥ 1V Iload= PWM Load	-2		2	%
Output Discharge Switch On Resistance				600	Ω
Buck – VS1					
Turn-on overshoot	No load			10	%
OCP(Over Current Protect)		Imax*1.2		5.75	A
Efficiency	VBAT=4.0V, Vout=2.1V, L_DCR.Max=53mΩ I_Load=50mA		90		%
	VBAT=4.0V, Vout=2.1V, L_DCR.Max=53mΩ I_Load=500mA		88		%
	VBAT=4.0V, Vout=2.1V, L_DCR.Max=53mΩ I_Load=1 A		87		%
	VBAT=4.0V, Vout=2.1V, L_DCR.Max=53mΩ I_Load=1.9 A		83		%
	VBAT=4.0V, Vout=2.1V, L_DCR.Max=53mΩ I_Load=2.5 A		84		%
Soft start	No load			1000	us
Switching Frequency	I_Load =1A	1.8	2	2.2	MHz
Output ripple voltage (PWM)	VBAT=3.8V,Vo=2.1V I_Load=0.5*Imax 20MHz measurement BW			13	mVp-p
Load transient	VBAT=3.8V I_Load= 1200mA <–> 1500mA (Tr/Tf=5us)	-4		5.5	%
Line transient	Vbat=3.8V to 4.5V I_Load= 0.5*Imax (Tr/Tf = 15us)	-4		5.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.15V to 5.0V I_Load=PWM Load	-0.9		0.9	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.15V to 5.0V I_Load=PFM Load	-0.9		4.1	%
Output Discharge Switch On Resistance				250	Ω

Table 2-6. LDO specifications

Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
Power source	ALDO and DLDO	VBAT voltage	max{Vo+0.3 5 ; 3.15}		5	V

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
	SLDO	VBAT voltage		3.15		5	V
	SLDO	VS1 = VS2 = 2.1V		max{Vo+0.15 ; 2.1*0.95}		2.1*1.05	V
Overall DC voltage accuracy	ALDO, DLDO and SLDO Normal mode	Default voltage		-1.5		+1.5	%
		Non default voltage		-3		+3	%
	ALDO, DLDO and SLDO Low power mode	All voltages		-4		+4	%
Load regulation	ALDO, DLDO and SLDO Normal mode	Iout = 0mA~Imax	1. Power source 2. Typical capacitor 3. TA= -40°C~+85°C	-1.5		+1.5	%
	ALDO, DLDO and SLDO Low power mode	Iout= 0mA~5mA		-4		+4	%
	VRTC, DVDD18_DIG	Iout = 0mA~0.2*Imax		-10		+10	%
Line regulation	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C	-1.5		+1.5	%
	VRTC, DVDD18_DIG	Iout = 0mA		-5		5	%
Power off voltage	ALDO, DLDO and SLDO	Iou t= 0mA	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C		0.1		V
Load transient response	ALDO	Iout = 1mA~0.5*Imax@ Slew rate = 15mA/us	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C	-4		+4	%
	DLDO and SLDO	Iout = 1mA~0.5*Imax@ Slew rate = 80mA/us					
Turn-on rise time	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			300	us
Turn-on overshoot	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			+10	%
Normal mode quiescent current	ALDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			55	uA
	DLDO					55	
	SLDO (Current loading					100	

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
	≦0.3A)						
	SLDO (0.3A<Current loading≦0.6A)					160	
	SLDO (Current loading > 0.6A)					220	
	VRTC and DVDD18_DIG					10	
Low power mode quiescent current	SLDO					15	
	ALDO, DLDO					10	
Power off time	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Capacitor ≦ 2.2uF 3. TA= 25°C			4	ms
			1. Power source 2. Capacitor ≦ 9.4uF 3. TA= 25°C			12	ms
Output noise	ALDO	Freq = 10Hz to 80kHz	1. Power source 2. Typical capacitor 3. TA= +25°C 4. Iout = 0.2*Imax~0.5*Imax		90		uVrms
	DLDO and SLDO				500		uVrms
	ALDO, DLDO and SLDO	Freq = 10Hz to 10MHz			1000		uVrms
PSRR	ALDO	Freq = 217Hz to 3kHz	1. Power source 2. Typical capacitor 3. TA= +25°C 4. Iout = 0.2*Imax~0.5*Imax		65		dB
		Freq= 3kHz to 30kHz			45		dB
	DLDO and SLDO	Freq = 217Hz			40		dB
Short current	ALDO, DLDO and SLDO	OC	1. Power source 2. Typical capacitor 3. TA= +25°C	1.2 x Imax		3 x Imax	A
		OCFB		0.2 x Imax		2 x Imax	A

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.7 Driver

Table 2-7. Driver specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
ISINK					
ISINK LED sink current	ISINK_SEL = 000		2		mA
	ISINK_SEL = 001		4		mA
	ISINK_SEL = 010		6		mA
	ISINK_SEL = 011		8		mA
	ISINK_SEL = 100		10		mA
	ISINK_SEL = 101		12		mA
ISINK dropout voltage	2 ~ 12mA VISINK drop			225	mV
ISINK rise/fall time	VISINK > 0.225V			3.33	uS
Pre-Charge Indicator					
LED sink current	VBUS=4.0~10.5V VBAT=2.2V~5V Visink=1.2V~2.8V		2		mA
			4		mA
			6(default)		mA
Dropout voltage	VBAT=2.2V-5V 2mA~6mA Visink drop			1.2	V
Rise/Fall time	Visink>1.2V			3.33	us
Breath mode two step rising/falling time	Two step corner rate		30		%
VIBR					
Output voltage	VIBR_SEL = 0000		1.2		V
	VIBR_SEL = 0001		1.3		V
	VIBR_SEL = 0010		1.5		V
	VIBR_SEL = 0100		1.8		V
	VIBR_SEL = 0101		2.0		V
	VIBR_SEL = 1001		2.8		V
	VIBR_SEL = 1011		3.0		V
	VIBR_SEL = 1101		3.3		V
Output current			200		mA

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.8 Audio CODEC

Table 2-8. Audio downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to audio buffer output (single-ended output, AU_HPL/R; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +5dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		23.4		mW
SNR (1)	Signal to noise ratio (A-weighted)		107		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-96 -97 -96		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-90 -94 -93		dB
NF_{OUT}	Output noise floor (A-weighted)		4		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		+8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
XT_{LR}	L/R channel crosstalk @1kHz		-110		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HPL/R) @ 1kHz		-96		dB
Glitch	Click-and-Pop (CnP) suppression		-80	-75	dBVpp (rms)
DC offset	Output DC offset measured at silent input			0.3	mV
DAC to audio buffer output (single-ended output, AU_HPL/R; R_{LOAD} = 16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +4dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		36		mW
SNR (1)	Signal to noise ratio (A-weighted)		107		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-92 -95 -94		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		-90 -93 -92		dB
NF_{OUT}	Output noise floor (A-weighted)		3.9		µVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Line-out Output (Differential Outputs, AU_LOLP/N; R_{LOAD} = 600)					

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +5dB, 24bit audio data					
V_{OUT}	Maximum output swing @<1% THD @PGA_{DL} gain =+5dB gain		4.7		dBV
SNR (1)	Signal to Noise Ratio (A-weighted)		109		dB(A)
THD	Total Harmonic Distortion (THD) @ PGA_{DL} gain =+5dB gain		-90		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 3.2mW		-90		dB
NF_{OUT}	Output Noise Floor (A-weighted)		5.12		µVrms (A)
R_{LOAD}	Output Resistor Load (headphone)		560		Ω
C_{LOAD}	Output Capacitor Load			500	pF
$APGR_{DL}$	Analog Programmable Gain Range	-10		+8	dB
$APGS_{DL}$	Analog Programmable Gain Step		1		dB
PSRR	Power Supply Rejection Ratio (from AVDD18_AUD to AU_LOLP/N) @ 1kHz		-96		dB

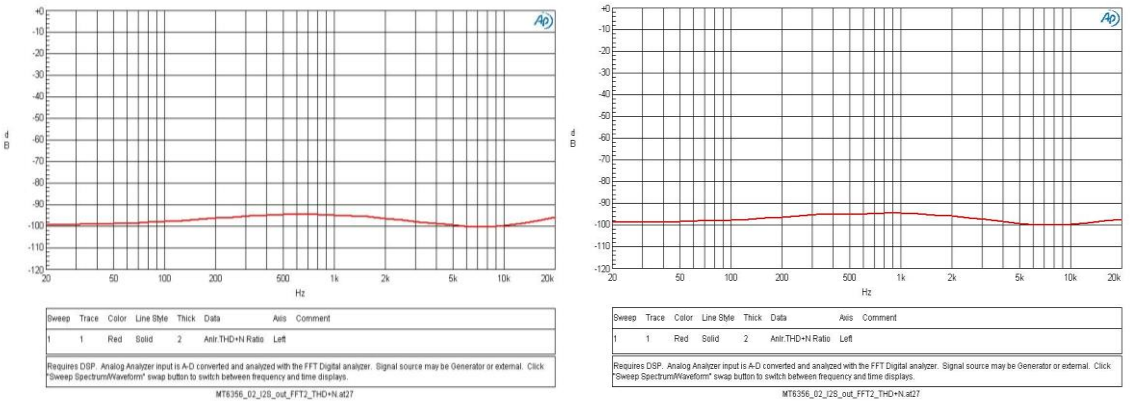
Note 1: Ratio of output level with 1kHz full-scale sine input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to voice buffer output (differential outputs, AU_HSP/N; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +5dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		88.5		mW
SNR (1)	Signal to noise ratio (A-weighted)		110		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -90 -90		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -90 -90		dB
NF_{OUT}	Output noise floor (A-weighted)		5.127		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		+8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HSP/N) @ 1kHz		-96		dB
DAC to voice buffer output (differential outputs, AU_HSP/N; R_{LOAD} =16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +4dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		129.8		mW
SNR (1)	Signal to noise ratio (A-weighted)		109		dB(A)
THD	Total harmonic distortion (THD) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -90 -90		dB
THD+N	THD Plus noise (THD+N) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -90 -90		dB
NF_{OUT}	Output noise floor (A-weighted)		4.9		µVrms

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

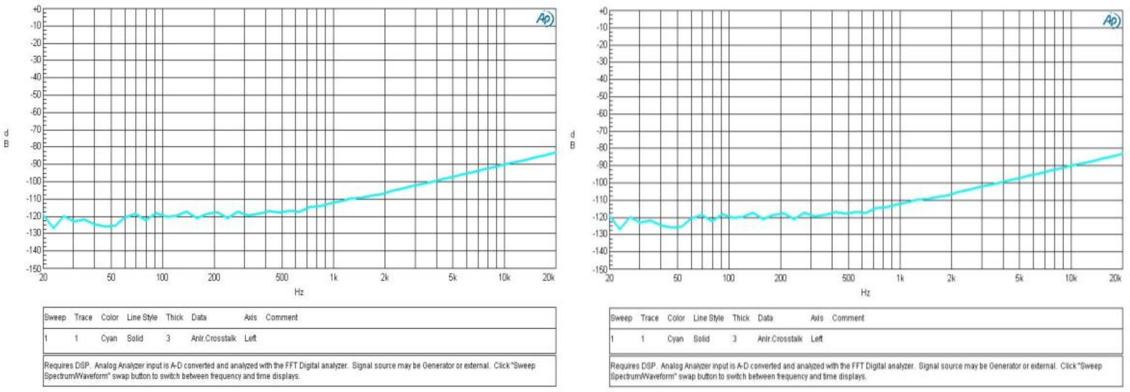
Symbol	Parameter	Min.	Typ.	Max.	Unit
					(A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]



(a) P_{OUT}=22.5mW (b) Pout=10mW

Figure 2-1. Audio Path THD+N vs. frequency



(a) Xtalk RtoL (b) Xtalk LtoR

Figure 2-2. Audio path Xtalk vs. frequency @P_{OUT}=10mW

Table 2-9. Audio uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue input paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-96		dB
N_{IN}	Input-referred noise		14.3		μVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-87		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-36		dB
Analogue input paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Symbol	Parameter	Min.	Typ.	Max.	Unit
SNR*1	Signal to noise ratio		-85		dB
N_{IN}	Input-referred noise		6.84		µVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-83		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-25		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue input paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-96		dB
N_{IN}	Input-referred noise		15.83		µVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-88		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-36		dB
Analogue Input Paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, FS,UL = 48kHz, PGAUL gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		-87		dB
N_{IN}	Input-referred noise		5.37		µVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-85		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-27		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured w/i A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer
Note 2: The input voltage range of AU_VIN0, AU_VIN1, and AU_VIN2 are within [AVDD28_AUD, AVSS28_AUD], and suggesting maximum input swing $V_{pp} \leq 1V_{rms}$ *(0 dBV) @* PGA_{UL} *gain = 0dB*

General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
$APGR_{UL}$	Uplink analog programmable gain range	0		24	dB
$APGS_{UL}$	Uplink analog programmable gain step		6		dB
CMRR	Common-mode rejection ratio @-18dBV, 1kHz sinusoid signal to both pins of an input configured differentially	40	75		dB
$XT_{Internal}$	ULL-to-ULR channel separation @ one input terminated with -18dBV, 1kHz sinusoid signal. Measure digital output of terminated channel	60	89		dB
XT_{DL2UL}	DL-to-UL channel separation @ 0dBV, 1kHz Rx path with RLOAD = 32	60	105		dB
PSRR	217Hz @ 200 mVpp square wave imposed on power. Measure digital output		-71		dB
	1kHz @ 200 mVpp square wave imposed on power. Measure digital output		-86		dB
	10kHz @ 200 mVpp square wave imposed on power. Measure digital output		-90		dB
$F_{S,UL}$	Audio uplink sampling rate 8, 16, 32, and 48kHz	8		48	KHz

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Digital MIC					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
DCLK	DMIC clock frequency	0.406	1.62	3.25	MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns

Table 2-10. MICBIAS specifications

Microphone Bias (MICBIAS) Temp = 25deg, 1μF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT}	Microphone bias voltage	1.7		2.6	V
V_{OUT} Step	Bias voltage output step size 1.7V~2.6V		0.1		V
I_{OUT}	Maximum output current (two MICBIAS loads total)			3	mA
N_{OUT}	Output integrated noise (20~20kHz A-weighted) with 1μF cap.		3.96		μVrms
PSRR	217Hz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
	1kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
	10kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		100		dB
$C_{LOAD,MIC}$	Output capacitor load on MICBIAS	0.1		22	μF

Table 2-11. ACCDET specifications

Accessory Detection (ACCDET)					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
-	*1: Load impedance detection range (ACCDET) by 1& 1.5kΩ (1%) MICBIAS resistors *2: The characteristics assume no other component is connected to ACCDET. *3: The key detection voltage will be normalized automatically. For different micbias settings, the same key (resistance is the same) is pressed, and the read voltage (key pressed) value will be similar.				
-	4-pole microphone detection	2k		14k	Ohm
Microphone impedance detection after 4-pole microphone plugged-in (for 3 key application)					
-	MICD_LVL[0]: Down key	400		620	Ohm
-	MICD_LVL[1]: Up key	150		320	Ohm
	MICD_LVL[2]: Hook key	0		100	Ohm

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.9 Battery Charger

Table 2-12. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN operating voltage		4	5	10.5	V
OTG B-Valid detection		0.8	2.4	4	V
VCDT CHRIN UVLO rising detection threshold	VCDT_VTHL[4:0] = 00010 ~ 01010	4.0		4.45	V
	Accuracy	-4.5		4.5	%
VCDT CHRIN UVLO falling detection threshold	Falling level for charger plug-out detection (default)		3.9		V
	Accuracy	-6		6	%
VCDT CHRIN OVP detection threshold	VCDT_VTHH[4:0] = 01011 ~ 10100	6		14	V
	Accuracy	-4.5		4.5	%
HV adaptive current @ pre_charge	CHRIN rising threshold for ICHG current change 300mA -> 70mA		7		V
	CHRIN falling threshold for ICHG current change 70mA -> 300mA		6		V
VBAT CC voltage accuracy	Programmable: 3.3~3.45, 50mV steps	-50		+50	mV
VBAT CV voltage accuracy	Programmable: 3.9~4.6 V	-30		+30	mV
VBAT OV voltage accuracy	Programmable: 4.2~4.7 V	-30		+30	mV
CC mode charging current accuracy	Programmable:500 ~2000 mA (Rsense=56mΩ)	-10		+10	%

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.10 BC1.2

Table 2-13. BC1.2 specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
BC12 charging port detection (Pre-CC current)	Standard down-stream port		70	100	mA
	Standard charging down-stream port		300		mA
	DP, DM short		300		mA
BC12 characteristics	DP, DM floating		300		mA
	IPU_DP, IPU_DM	7	9.6	13	uA
	IPD_DP, IPD_DM	50	96	150	uA
	VSRC on DP, DM	500	630	700	mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms
	OSC1M, timer		5		min

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.11 Down Load Without Battery

Table 2-14. Download without battery specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		32.0		s
	Current		450		mA

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.12 AUXADC

Table 2-15. AUXADC specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage		-	1.8	-	V
Resolution	Channel 0,1,7	-	-	15	Bits
	Others	-	-	12	Bits
Analog-input bandwidth			50K		Hz
Sample rate			100K		Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output		2		LSB
DNL	15-bit output		2		LSB

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.13 Fuel Gauge

Table 2-16. Fuel gauge specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/16		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		2.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2.14 DCXO

Table 2-17. XO specification

Parameter	Condition	Title	Min.	Typ.	Max.	Unit
Supply current in suspend (OSC LPM)	VXO22=2.2V; without 32K RTC	$I_{xo,lpm}$		75		uA
Supply current in idle (OSC + one buffer for SOC)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,idle}$		1.5		mA
Supply current in RF TRx (OSC + buffers for SOC, RF_Cell)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,trx}$		4.6		mA
Extra supply current for RF_Conn	VXO22=2.2V; PCB Cload<20pF	$I_{xo,conn}$		2		mA
Extra Supply current for RF_NFC or RF_EXT	VXO22=2.2V; PCB Cload<20pF	$I_{xo,nfc}$		1		mA
Leakage current	VXO22=2.2V; with 32K RTC	$I_{xo,leak}$			1	uA
Center operating frequency	Internal resonant; with QVL crystal	F_{dcxo}		26		MHz
Duty cycle	Square wave in high driving mode		45	50	55	%
Static tuning range	XTAL1/2 differential input capacitance	C_{TR}	4.0		8.5	pF
CapID binary bits	CDAC			8		bit
Startup time, after clock request	Delta f < 1ppm.	$T_{startup}$		1	2	ms
Crystal input pins	Specific foundries			2		pin
Crystal size	CL=7~7.5pF		2016	2520	3225	

Table 2-18. Reference input buffer specification (XTAL1, buffer mode)

Parameter	Conditions	Min.	Nom.	Max.	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	3	5		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		5	10	pF

This pin should be AC coupled when used with an external clock source.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3 Functional Descriptions

3.1 General Descriptions

MT6357 is a fully integrated PMIC target for smart phone power provider. The following is the block diagram of MT6357 PMIC.

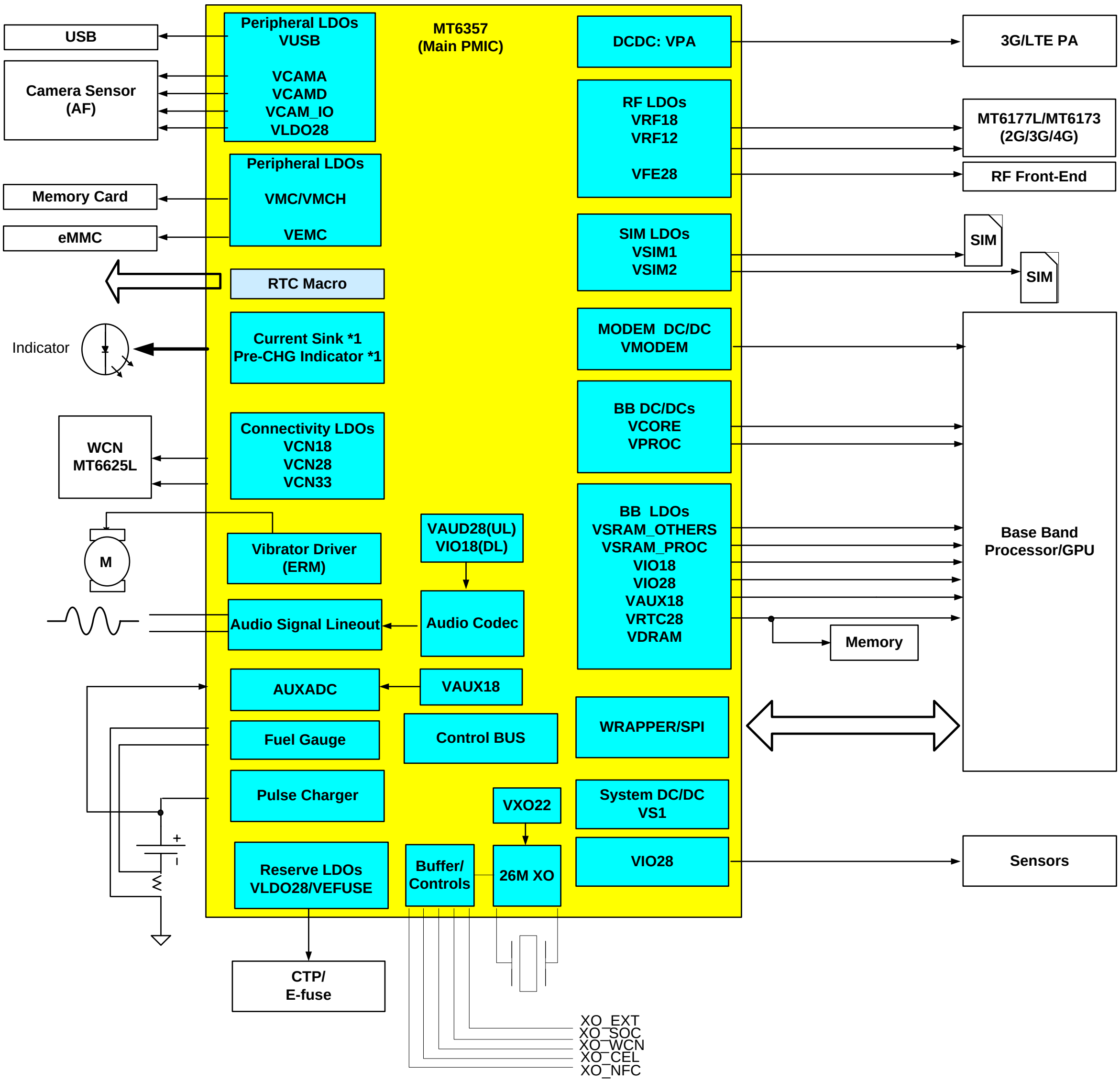


Figure 3-1. MT6357 block diagram

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2 PMIC Functional Blocks

MT6357 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6357 includes the following analog functions for use on smart phone platforms.

- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Current sink (ISINK) driver: Sink current for indicator
- Vibrator driver: Provides regulated power for vibrator.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Charger controller: Controls/Protects battery charging procedure
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- Fuel gauge: Supports accurate battery capacity monitor

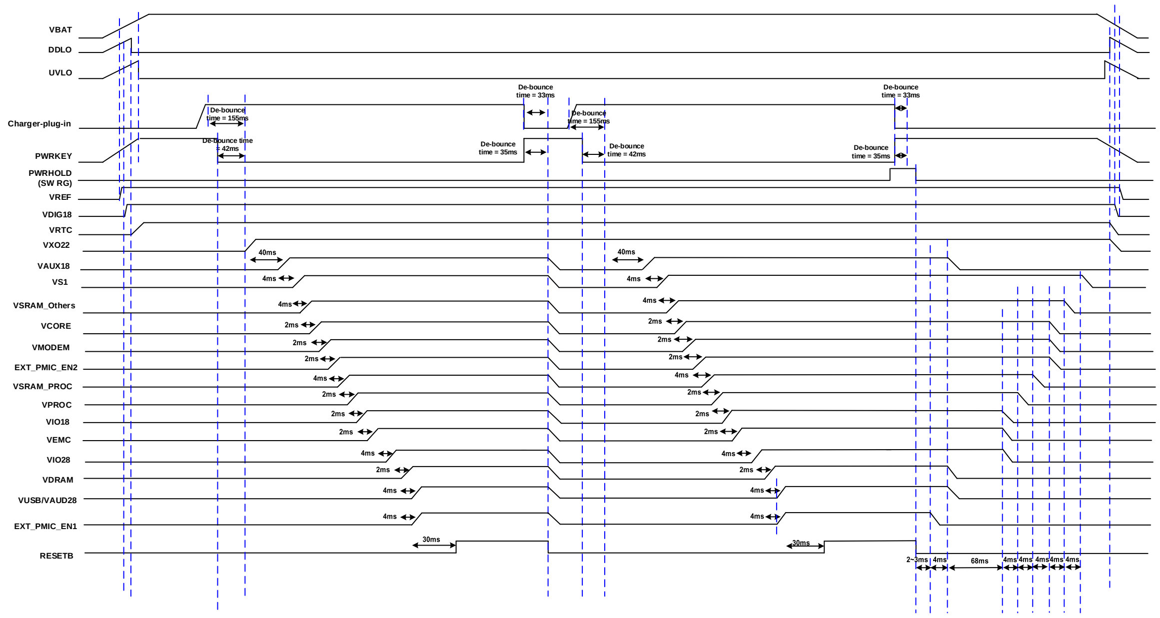
More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state nor in the thermal condition, there are four methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY.)
2) Valid charger plug-in
3) ALARM
4) SPAR

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.



Note: Those timings are typical values; timing variation is +-20%(Charger-plug-in/out related delay timing variation is +-40%).

Figure 3-2. Power-on/off control sequence without XTAL by charger plug in or by pressing PWRKEY

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the PWRHOLD signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives PWRHOLD from the baseband.

2. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage is inside valid range between CHGIN_VTHL and CHGIN_VTHH and VSYS > UVLO, the handset will also be powered on.

3. RTC module generates ALARM to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the ALARM signal will be directly sent to PMIC. In this case, ALARM becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

4. RTC module generates SPAR to power on the system. When the sudden power drops to less than the pre-defined time period during system on and the VSYS returns to above UVLO, SPAR will be held high to allow PMIC to power on.

Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VSYSSNS. It ensures that the handset is powered on with the

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC28 and VXO22 LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. VRTC28 and VXO22 LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)
PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC28 and VXO22 LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset
PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection
If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC28 and VXO22. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are five buck converters in MT6357 to efficiently generate regulated power for graphic processor, digital core and other block. Figure 3-1 is the block diagram. The buck converters operate with 2MHz (VS1 buck and VPA) fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. Only VPROC/VCORE/VMODEM bucks operate with 2.2MHz on Constant-On Time(COT) mode to improve mode/load transition performance. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up. For each buck converter, there is also included auto discharging path inside switching node to confirm there won't have any remainder voltage when turned off buck. The maximum discharge resistance value are 50Ω (VPROC/VCORE)/120Ω (VMODEM)/250Ω (VS1) /600Ω (VPA) respectively.

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Table 3-1. Buck converter brief specifications

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VPROC	1.15	0.51875~ 1.31	6.25	4210	Y	PROCESSOR
VCORE	1.15	0.51875 ~ 1.2	6.25	3500	Y	Digital core always on
VMODEM	1.15	0.65 ~ 1.2	6.25	2,000	Y	MODEM
VS1	2.1	1.86~2.2	12.5	2,500	Y	SYS LDOs power
VPA	0.5	0.5~3.4	50	1000(1)	N	RF PA

Note:

1. Due to PA application is resistance load and $R_{PA,MIN}$=4.5ohm.
   So the VPA IMAX is determined as following equation: VOUT/ $R_{PA,MIN}$ except IMAX=1000mA when VOUT≥3.4V

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power domain	Controller power domain	Default Voltage (V)	Imax (mA)	Application
ALDO	VFE28	VSYS_LDO2	VSYS_LDO2	2.8	50	RF AFE
ALDO	VXO22	VSYS_LDO3	VSYS_LDO3	2.24	25	DCXO
SLDO	VRF18	VS1_LDO1	VSYS_LDO1	1.81	450	RF
SLDO	VRF12	VS2_LDO2	VSYS_LDO1	1.2	400	RF
DLDO	VEFUSE	VSYS_LDO1	VSYS_LDO1	1.8	200	EFUSE
DLDO	VCN33	VSYS_LDO2	VSYS_LDO2	3.5	400	Connectivity
ALDO	VCN28	VSYS_LDO2	VSYS_LDO2	2.8	50	Connectivity
SLDO	VCN18	VS1_LDO1	VSYS_LDO1	1.8	300	Connectivity
ALDO	VCAMA	VSYS_LDO1	VSYS_LDO1	2.8	200	Camera analog power
SLDO	VCAMIO	VS1_LDO1	VSYS_LDO1	1.8	300	Camera IO power
SLDO	VCAMD	VS2_LDO1	VSYS_LDO1	1.2	300	Camera digital power
DLDO	VLDO28	VSYS_LDO1	VSYS_LDO1	2.8	400	1. Camera AF 2. Touch Panel
ALDO	VAUX18	VSYS_LDO3	VSYS_LDO3	1.8	50	AUXADC
ALDO	VAUD28	VSYS_LDO3	VSYS_LDO3	2.8	50	Audio
DLDO	VIO28	VSYS_LDO1	VSYS_LDO1	2.8	200	IO and sensor
SLDO	VIO18	VS1_LDO1	VSYS_LDO1	1.8	600	IO and eMMC
SLDO	VSRAM_PROC	VS2_LDO2	VSYS_LDO1	1.25	200	SRAM
SLDO	VSRAM_OTHERS	VS2_LDO2	VSYS_LDO1	1.25	200	SRAM
SLDO	VDRAM	VS2_LDO2	VSYS_LDO1	1.24	1200	DRAM
DLDO	VMC	VSYS_LDO2	VSYS_LDO2	3	200	MSDC
DLDO	VMCH	VSYS_LDO2	VSYS_LDO2	3	800	SD card
DLDO	VEMC	VSYS_LDO1	VSYS_LDO1	3	400	eMMC and UFS

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Type	LDO name	Input power domain	Controller power domain	Default Voltage (V)	Imax (mA)	Application
DLDO	VSIM1	VSYS_LDO1	VSYS_LDO1	1.86	200	SIM1 card
DLDO	VSIM2	VSYS_LDO1	VSYS_LDO1	1.86	200	SIM2 card
DLDO	VIBR	VSYS_LDO2	VSYS_LDO2	2.8	200	Vibrator
DLDO	VUSB	VSYS_LDO1	VSYS_LDO1	3.07	200	USB power
VRTC	VRTC28	VSYSSNS	VSYSSNS	2.8	2	RTC macro
VDIG	DVDD18_DIG	VSYSSNS	VSYSSNS	1.8	10	PMIC internal digital power
Power Switch	TREF	VAUX18	BATSNS	1.8	1	Battery interface

3.2.4 Drivers

MT6357 supports 1 channel indicator LED drivers. The following figure depicts the major application for indicator LEDs drivers. The LED driver of MT6357 supports PWM/Register/Breath mode.

When the LED current is from small to large then descends, it is the breath mode. Through software programming the registers in Figure 3-4, MT6357 can change the breathing cycle time, including Tr1, Tr2, Ton, Toff, Tf1 and Tf2 period.

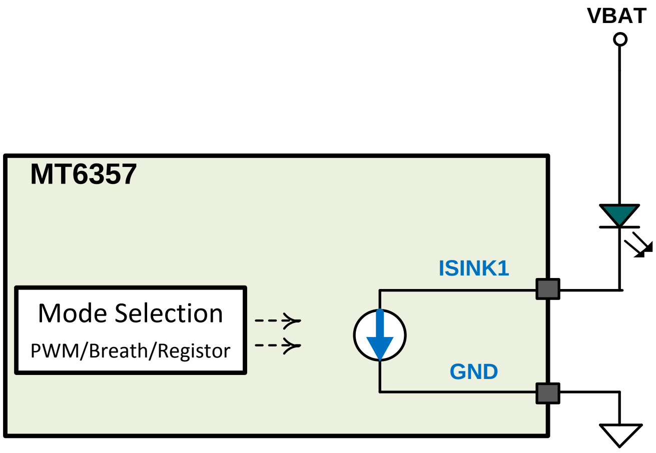


Figure 3-3. Configuration for indicator LED drivers

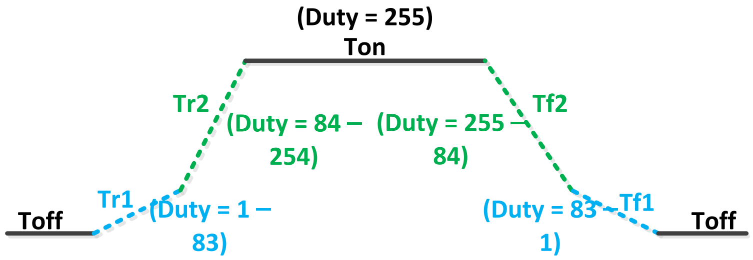


Figure 3-4. LED drivers breath mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2.5 Pre-Charge Indicator

MT6357 supports an independent indicator LED driver (pre-charge indicator). Once the charger is plugged in, the indicator will be always on to indicate the system is being charged. After the software works with the existing charger, it will have the same function as other LED drivers do.

3.2.6 Vibrator Driver

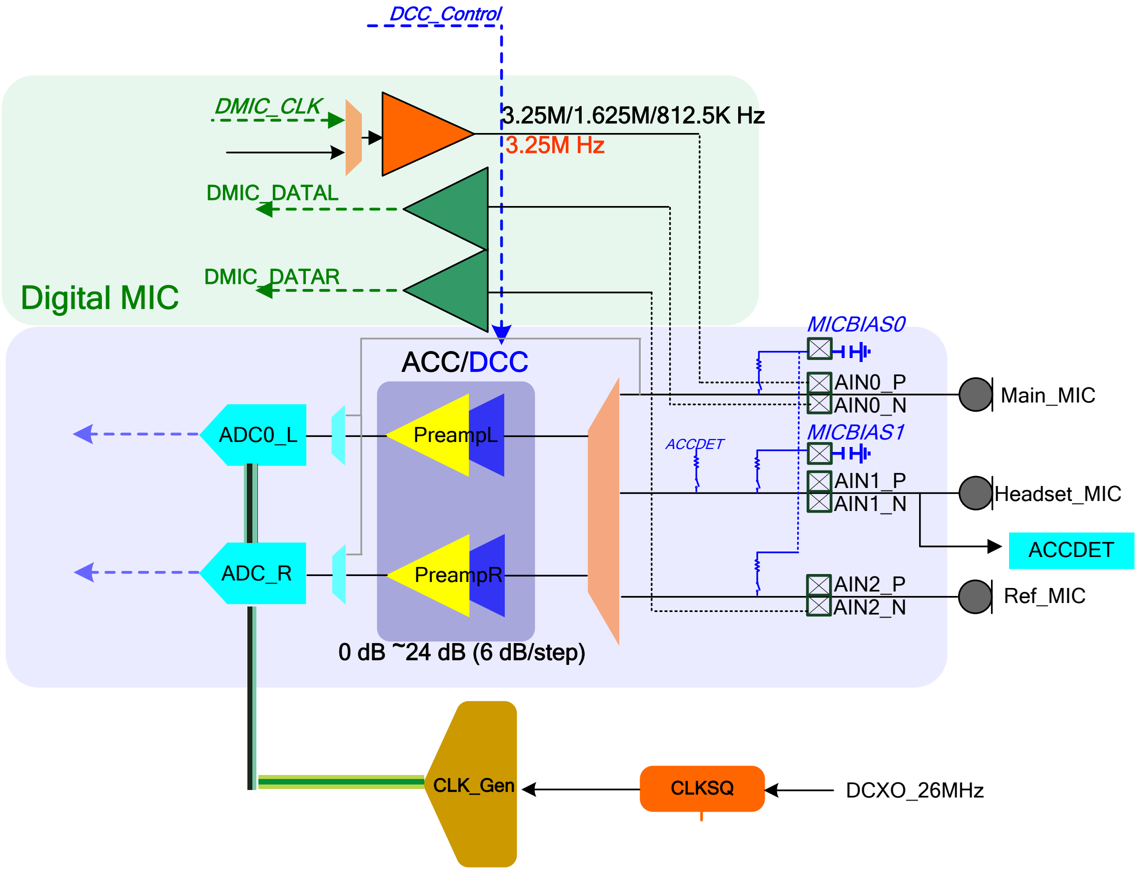
The VIBR driver power allows up to 100mA current for ERM (Eccentric Rotating Mass) or coin type vibrator with programmable output voltage.

3.2.7 Audio CODEC and Accessory Detection

3.2.7.1 Block Descriptions

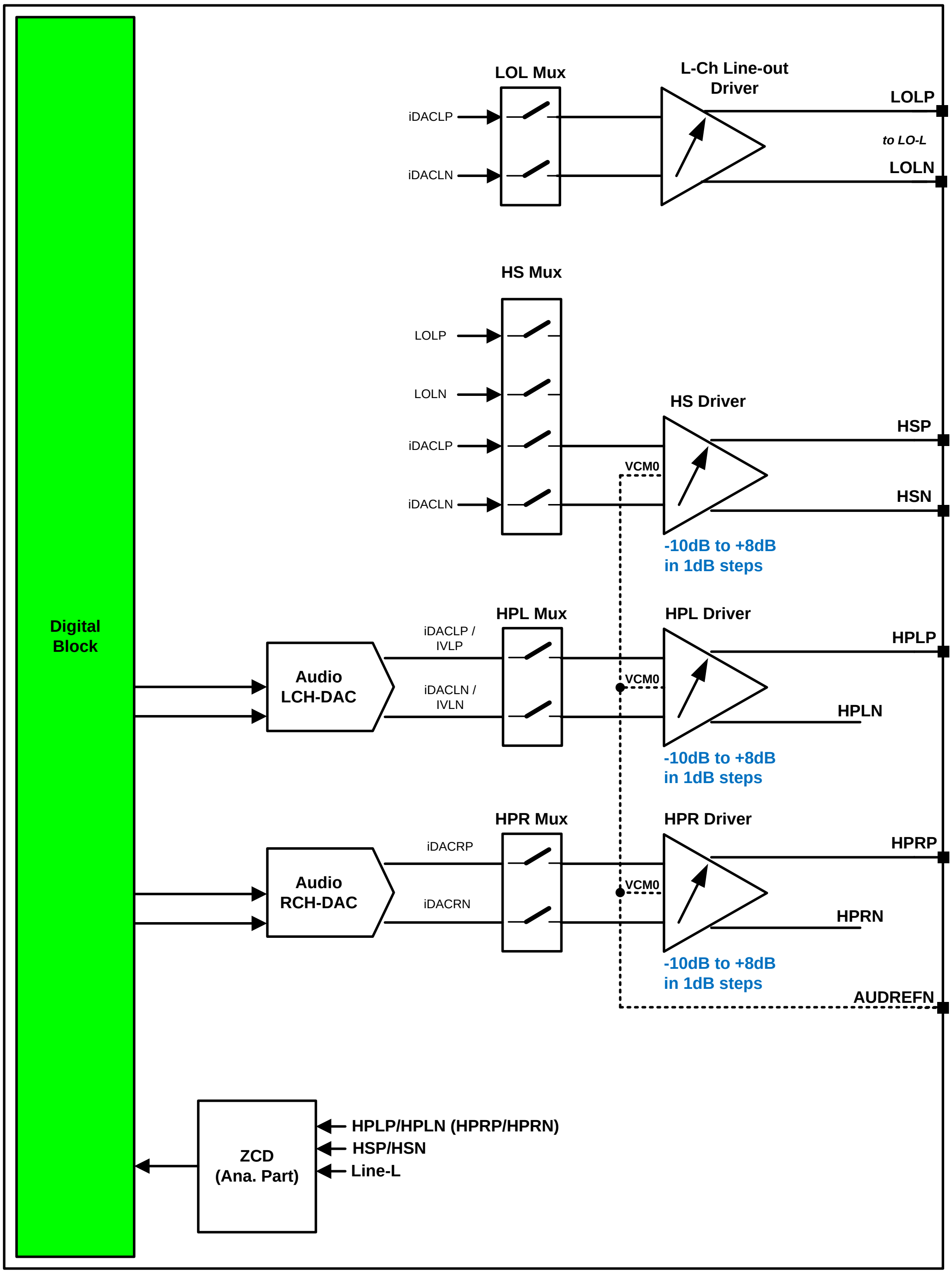
The block diagram of audio codec is illustrated below. The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC, and digital MIC. The uplink front-end to PGA can be configured as ACC or DCC type. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and a mono voice driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The internal high output power loud-speaker amplifier is also embedded. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.



(a) Audio/speech uplink and accessory detection

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.



(b) Audio/speech downlink

Figure 3-5. Audio CODEC block diagram

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2.8 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

3.2.8.1 Block Descriptions

Block diagram of battery charger:

Charger block diagram

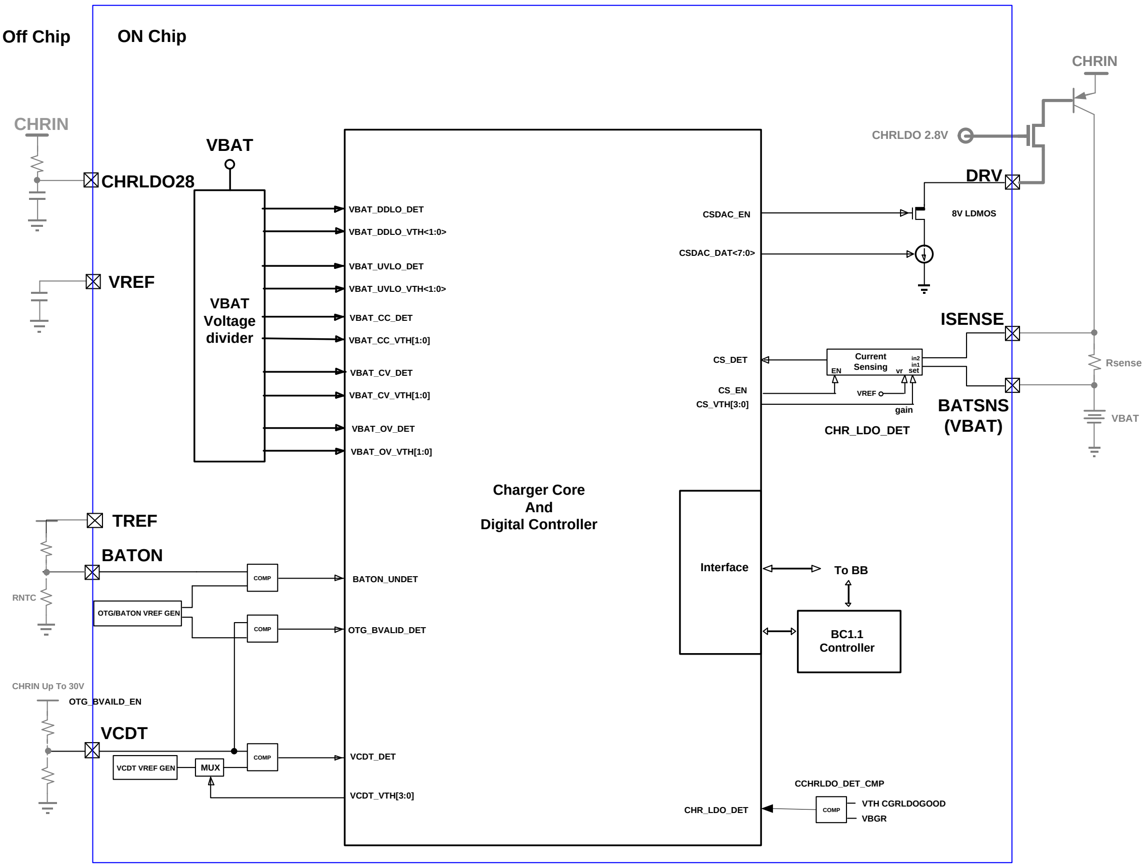


Figure 3-6. Block diagram of battery charger

3.2.8.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V, software default setting), the charger detector will stop the charging process immediately to avoid burning out the chip or even the phone. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2.8.1.2 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.0V, PMIC power-off state), CC mode (Constant Current mode or fast charging mode at the range of 3.0V < VBAT < 4.2V, CV default voltage) and CV mode (Constant Voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

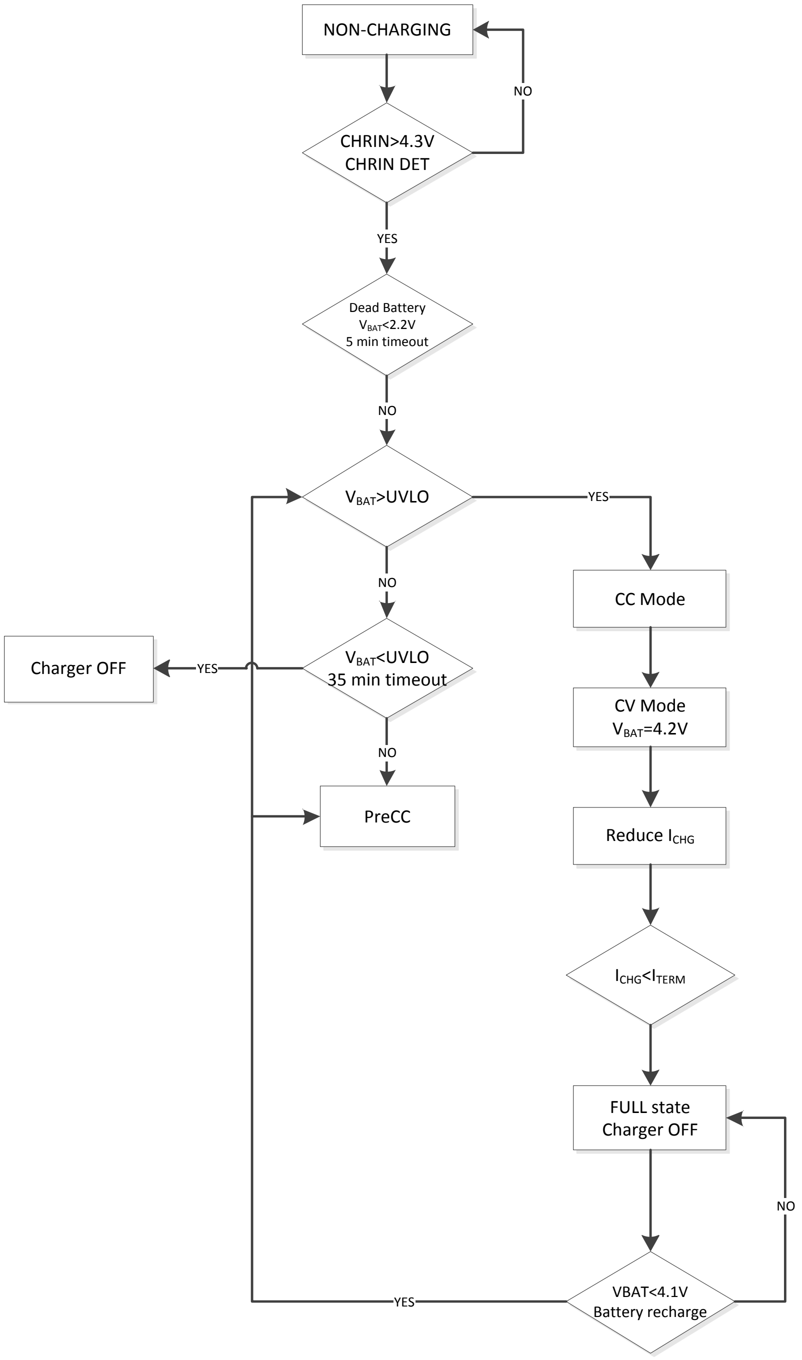


Figure 3-7. Flow chart of charging states

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 16.8mV (AC charger) or 3.92mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,\ AC\ adapter} = \frac{V_{SENSE}}{Rsense} = \frac{16.8mV}{Rsense}$$

$$I_{PRECC1,\ USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{3.92mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.0V, it can switch to the CC mode (CHR_EN should be high.) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.056Ω, the CC mode charging current can be set from 70mA to 2,000mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant-voltage mode and over-voltage protection (OV)

When the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. When the battery voltage actually reaches 4.2V, the charging current gradually decreased step-by-step, and the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches termination current automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection will be activated and turns off the charger immediately.

3.2.8.1.3 BC1.2 Dead-Battery Support

MT6357 also supports dead-battery condition BC1.2. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after the trickle current is applied, the charger will be disabled. On the other hand, once the battery voltage rises to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

When the battery is below 3.0V, the charger will charge the battery by the PRECC1 current.

A dedicated 5 min. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35 min. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.45V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.2.8.1.4 Auto Power-On Mode (USB Download without Battery)

MT6357 features a default auto power-on mode (or USB DL without battery) no matter with or without battery. You can disable auto power-on by adding external pull-high resistor on the FCHR_ENB pin. USB DL (auto power-on) can still be initiated by pressing DL_KEY or under valid BAT_ON information (decided by customers' PCB options). Nonetheless, DL_KEY supports key function in normal mode. The valid BAT_ON information can be detected through the battery's NTC when it is connected to pin BAT_ON of MT6357.

3.2.9 AUXADC

3.2.9.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data..

Table 3-3. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.5
1	ISENSE	2.5 ~ 4.5
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 1.7
5	ACCDET	0 ~ 1.8
7	AUXADC_VIN	0 ~ 1.8
others	Internal use	N/A

3.2.10 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to convert the current drawn from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

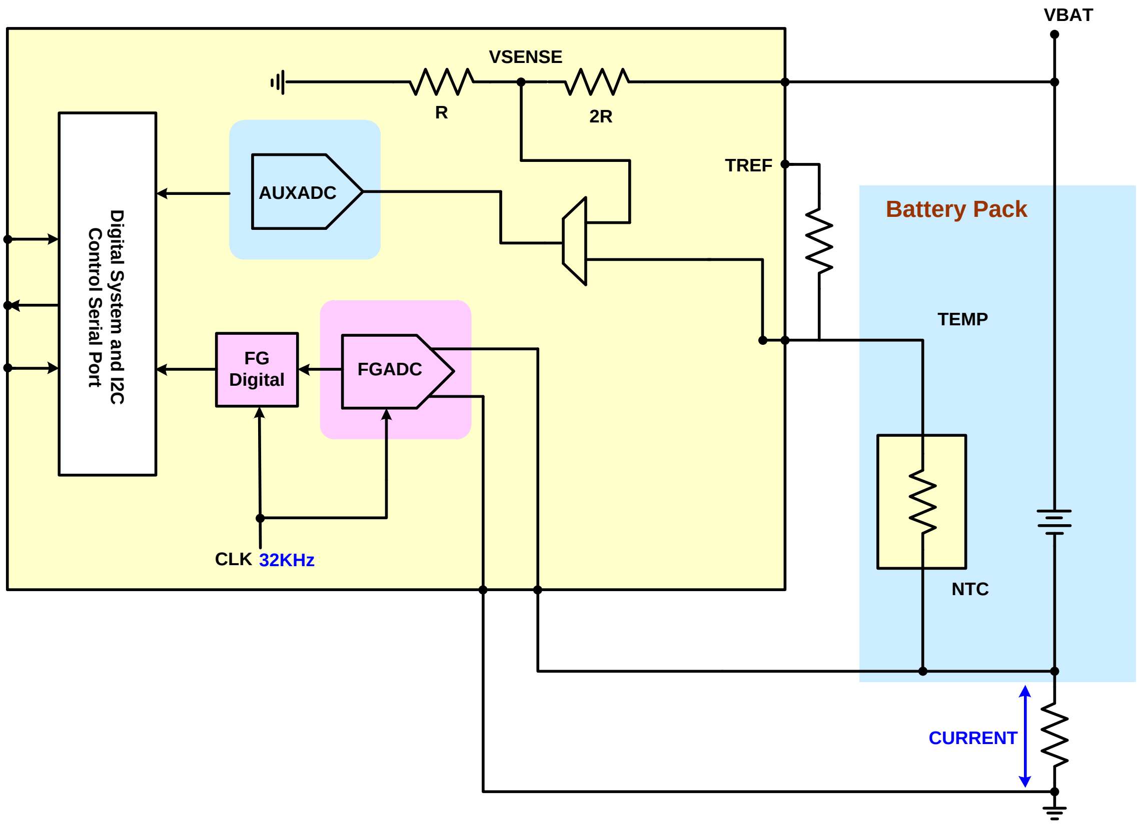


Figure 3-8. Fuel gauge block diagram and external connection

3.2.11 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on 32kHz from DCXO or an embedded 32kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6357, RTC module only supports function without 32kHz crystal. RTC module has an embedded 32kHz oscillator to assist life time extension after DCXO 32kHz clock is off.

3.2.12 DCXO

3.2.12.1 Reference Clock Specification

MT6357 PMIC integrates a core 26MHz XTAL oscillator (XO) and supports 32kHz RTC-removal low power mode. It also provides backward compatible (BCM) configurations for previous solutions. There are two High Performance (1.8V_{PP}) and three Low Power (1.0V_{PP}) external clock buffers for the entire system and one internal buffer for audio.

The modes of operation are configured by two input pins, DCXO32K_EN and XMODE, and the definitions are shown as below.

DCXO32K_EN	XMODE	Mode
LOW	LOW	Buffer mode with external TCXO
LOW	HIGH	Oscillator mode with 32K RTC
HIGH	LOW	BC M mode, system clock from RF
HIGH	HIGH	Oscillator mode without 32K RTC

In oscillator mode, the Temperature Sensing Crystal (TSX) is connected between XTAL1 and XTAL2. In buffer mode, the external clock inputs from XTAL1. Keep XTAL2 pin NC.

Note that DCXO32K_EN and XMODE are default high and can be programmed after the first power-on; after that MT6357 can select proper power-on-sequence for different system configurations.

3.2.12.2 Reference Output Buffer(s) Specification

There are five 26MHz clock output buffers driving out from the chip. They can be used as reference clocks for other chips and applications. Two High Performance (HP) external buffers output 0~1.8V squarer wave, and three Low Power (LP) external buffers output 0~1.0V squarer wave. Note that all their DC common mode voltage is not 0, so DC block capacitor is required if it is AC coupled and specific common mode voltage.

The current of all buffers can be optimized for different PCB Cloadings. Typical current consumption is optimized for < 20pF Cloading.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty cycle		40		60	%
Rise/Fall time	10% to 90% of signal swing @ Cload=20pF			5	ns
HP buffer output	Square wave	1.6	1.8	2.0	Vp-p
HP SSB phase noise	1Hz offset [20pF load]			-50	dBc/Hz
	5Hz offset [20pF load]			-73	dBc/Hz
	10Hz offset [20pF load]			-80	dBc/Hz
	100Hz offset [20pF load]			-106	dBc/Hz
	1kHz offset [20pF load]			-134	dBc/Hz
	10kHz offset [20pF load]			-144	dBc/Hz
	100kHz offset [20pF load]			-152	dBc/Hz
HP current consumption	Zload = 20pF (each buffer)		2.0		mA
LP buffer output	Square wave	0.8	1.1	1.3	Vp-p
LP SSB phase noise	100Hz offset [20pF load]			-85	dBc/Hz
	1kHz offset [20pF load]			-110	dBc/Hz
	10kHz offset [20pF load]			-130	dBc/Hz
	100kHz offset [20pF load]			-130	dBc/Hz
LP current consumption	Zload = 20pF (each buffer)		1		mA

3.2.12.3 32kHz RTC Removal Mode

In low power mode a 32kHz clock is produced by a fractional-N divider (1st order Sigma Delta Modulated) to replace the traditional 32kHz XTAL. The capacitance is minimized for significant current reduced.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Frequency	Averaged value		32768		Hz
XO LPM current consumption	Low power mode With all capacitors switched off and auto-amplitude calibration on		75		µA
Duty cycle				70	%
Settling time				5	ms
Frequency variation	After system calibration			±2	ppm
	Over temperature -30°C to 85°C			15	ppm
	Uncalibrated – total variation			200	ppm

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2.13 Interrupt and Watchdog

3.2.13.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - FCHR_ENB: Interrupt is issued when FCHR_ENB is pressed (and released, set by the register). After receiving the interrupt, the software will read the HOMEKEY _DEB status to see if it is pressed or released.
2. Charger related interrupt
3. Battery voltage/current H/L interrupt
   If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.
4. Fuel-gauge
5. Buck OC interrupt
   There are five bucks and each has its individual interrupt which uses PWM detection method.
6. Buck PREOC interrupt
   There are one buck preoc interrupts for VCORE.
7. LDO OC interrupt
   PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.
8. RTC interrupt
9. AUDIO interrupt
   Audio interrupt can inform AP playback of the audio status.
10. ACCDET interrupt
    This is for headphone detection.
11. Novel Adaptive Fuel Gauge (NAFG) delta-V accumulation interrupt
    If the accumulation of NAFG delta-voltage is larger than the programmable threshold, this interrupt will be issued.

3.2.13.2 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.13.3 Booting Watchdog Reset

PMIC implements a booting watchdog function to prevent AP not booting up correctly. After all default on powers are turned on and RESETB is released, WDTRSTB_IN or PWRHOLD should be set

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

high in a pre-determined time period or PMIC will shut down all powers and re-power on again if the PWRKEY or CHRIN power-on condition still exists.

3.2.14 SPI Interface

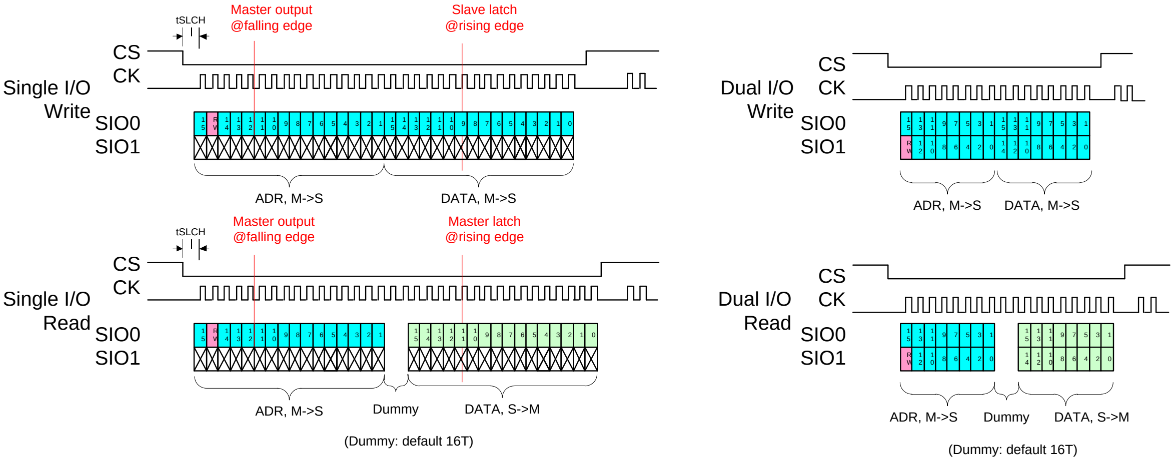
PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

3.2.14.1 Data Format

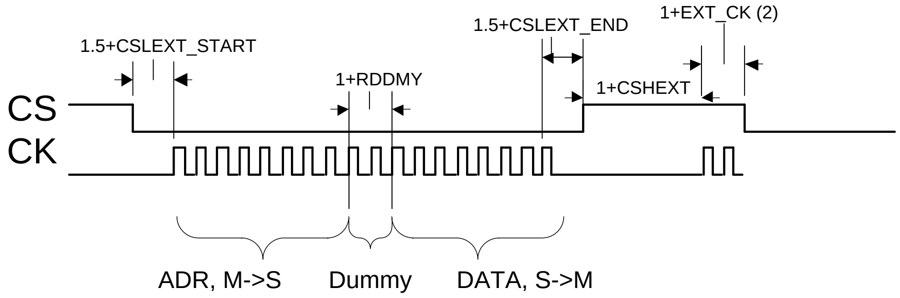
The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit15 to bit1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master is at the rising edge of the clock, and output data are at the falling edge of the clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

SPI parameter configuration:



 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2.15 GPIO

3.2.15.1 GPIO List

Table 3-7. MT6357 GPIO list

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
PAD_SRCLKEN_IN0	GPIO0	**I1:SRCLKEN_IN0**					I0:TEST_IN0	O:TEST_OUT0	**PU**/PD
PAD_SRCLKEN_IN1	GPIO1	**I1:SRCLKEN_IN1**					I0:TEST_IN1	O:TEST_OUT1	**PU**/PD
PAD_RTC32K_1V8_0	GPIO2	**O:RTC_32K1V8_0**					I0:TEST_IN2	O:TEST_OUT2	PU/PD
PAD_RTC32K_1V8_1	GPIO3	**O:RTC_32K1V8_1**	O:INT_1		I0: EINT0		I0:TEST_IN3	O:TEST_OUT3	PU/PD
PAD_SPI_CLK	GPIO4	**I0:SPI_CLK**							PU/**PD**
PAD_SPI_CSN	GPIO5	**I1:SPI_CSN**							**PU**/PD
PAD_SPI_MOSI	GPIO6	**B0:SPI_MOSI**							PU/PD
PAD_SPI_MISO	GPIO7	**B0:SPI_MISO**							PU/PD
PAD_AUD_CLK_MOSI	GPIO8	**I0:AUD_CLK_MOSI**				I0:TEST_CK0			PU/**PD**
PAD_AUD_DAT_MOSI0	GPIO9	**I0:AUD_DAT_MOSI0**					I0:TEST_IN4	O:TEST_OUT4	PU/**PD**
PAD_AUD_DAT_MOSI1	GPIO10	**I0:AUD_DAT_MOSI1**					I0:TEST_IN5	O:TEST_OUT5	PU/**PD**
PAD_AUD_SYNC_MOSI	GPIO11	**I0:AUD_SYNC_MOSI**					I0:TEST_IN6	O:TEST_OUT6	PU/**PD**
PAD_AUD_CLK_MISO	GPIO12	**O:AUD_CLK_MISO**					I0:TEST_IN7	O:TEST_OUT7	PU/PD
PAD_AUD_DAT_MISO0	GPIO13	**O:AUD_DAT_MISO0**	O:VOW_DAT_MISO	I0: DUMMY0					PU/PD
PAD_AUD_DAT_MISO1	GPIO14	**O:AUD_DAT_MISO1**		I0: DUMMY1		I0:TEST_CK1			PU/PD
PAD_AUD_SYNC_MISO	GPIO15	**O:AUD_SYNC_MISO**				I0:TEST_CK2			PU/PD

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.2.15.2 GPIO Specification

Table 3-8. MT6357 GPIO electrical characteristics

Paramters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.75*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.25*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH (DC)	DC Output logic low voltage	0.75*VDDQ			V
VOL (DC)	DC Output logic high voltage			0.25*VDDQ	V
Leakage					
IIN	Input leakage current (any input 0V < VIN < VDDIO)	-5		5	mA
IOZ	Tri-state output leakage current	-5		5	mA
IIN	Input leakage current (VIN=3.3V/0V) for floating nwell IO	-10		10	mA
IOZ	Tri-state output leakage current for for floating nwell IO	-10		10	mA

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

3.3 Register Table and Descriptions

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register Function
000C	PONSTS	16	Power On Source Record Register
000E	POFFSTS	16	Power off source record register
0010	PSTSCTL	16	Power On/Off Status Control
0014	PG_SDN_STS0	16	Power Good Shutdown Status 0
0016	OC_SDN_STS0	16	OC Shutdown Status 0
014C	TOP_RST_MISC	16	Reset Control Misc
019E	TOP_INT_STATUS0	16	TOP_INT_STATUS Register 0
038E	TOP_CLK_TRIM	16	TOP_CLK_TRIM Register
0390	OTP_CON0	16	OTP Control Register 0
0392	OTP_CON1	16	OTP Control Register 1
0394	OTP_CON2	16	OTP Control Register 2
0396	OTP_CON3	16	OTP Control Register 3
0398	OTP_CON4	16	OTP Control Register 4
039A	OTP_CON5	16	OTP Control Register 5
039C	OTP_CON6	16	OTP Control Register 6
039E	OTP_CON7	16	OTP Control Register 7
03A0	OTP_CON8	16	OTP Control Register 8
03A2	OTP_CON9	16	OTP Control Register 9
03A4	OTP_CON10	16	OTP Control Register 10
03A6	OTP_CON11	16	OTP Control Register 11
03A8	OTP_CON12	16	OTP Control Register 12
03AA	OTP_CON13	16	OTP Control Register 13
03AC	OTP_CON14	16	OTP Control Register 14
0514	SCK_TOP_CKPDN_CON0	16	SCK_CKPDN Control Register 0
0516	SCK_TOP_CKPDN_CON0_SET	16	SCK_CKPDN Control Register 0 SET
0518	SCK_TOP_CKPDN_CON0_CLR	16	SCK_CKPDN Control Register 0 CLR
051A	SCK_TOP_CKHWEN_CON0	16	SCK_CKHWEN Control Register 0
051C	SCK_TOP_CKHWEN_CON0_SET	16	SCK_CKHWEN_CON Register 0 SET
051E	SCK_TOP_CKHWEN_CON0_CLR	16	SCK_CKHWEN_CON Register 0 CLR
0528	SCK_TOP_INT_CON0	16	SCK_TOP INT Control Register 0
052E	SCK_TOP_INT_MASK_CON0	16	SCK_TOP INT mask Control Register 0
0534	SCK_TOP_INT_STATUS0	16	SCK_TOP INT Status Register 0
0538	SCK_TOP_INT_MISC_CON	16	SCK_TOP INT MISC Control Register
0588	RTC_BBPU	16	Baseband Power Up
058A	RTC_IRQ_STA	16	**RTC IRQ Status**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
			This register is fixed at 0 when RTC_POWERKEY1 and RTC_POWERKEY2 unmatch correct values.
058C	**RTC_IRQ_EN**	16	**RTC IRQ Enable** This register is fixed at 0 when RTC_POWERKEY1 and RTC_POWERKEY2 unmatch correct values.
058E	**RTC_CII_EN**	16	**Counter Increment IRQ Enable** Activates or de-activates the IRQ generation when the TC counter reaches its maximum value.
0590	**RTC_AL_MASK**	16	**RTC Alarm Mask** The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in this register is masked. Warning: If you set all bits 1 in RTC_AL_MASK (i.e. RTC_AL_MASK=0x7f) and PWREN=1 in RTC_BBPU, it means alarm comes every second, not disabled.
0592	**RTC_TC_SEC**	16	RTC Seconds Time Counter Register
0594	**RTC_TC_MIN**	16	RTC Minutes Time Counter Register
0596	**RTC_TC_HOU**	16	RTC Hours Time Counter Register
0598	**RTC_TC_DOM**	16	RTC Day-of-Month Time Counter Register
059A	**RTC_TC_DOW**	16	RTC Day-of-Week Time Counter Register
059C	**RTC_TC_MTH**	16	RTC Month Time Counter Register
059E	**RTC_TC_YEA**	16	RTC Year Time Counter Register
05A0	**RTC_AL_SEC**	16	RTC Second Alarm Setting Register
05A2	**RTC_AL_MIN**	16	RTC Minute Alarm Setting Register
05A4	**RTC_AL_HOU**	16	RTC Hour Alarm Setting Register
05A6	**RTC_AL_DOM**	16	RTC Day-of-Month Alarm Setting Register
05A8	**RTC_AL_DOW**	16	RTC Day-of-Week Alarm Setting Register
05AA	**RTC_AL_MTH**	16	RTC Month Alarm Setting Register
05AC	**RTC_AL_YEA**	16	RTC Year Alarm Setting Register
05AE	**RTC_OSC32CON**	16	**OSC32 Control** The function is only active when RTC_POWERKEY1 and RTC_POWERKEY2 match the correct values. When powerkeys do not match, the internal xosccali=0x7.
05B0	**RTC_POWERKEY1**	16	RTC_POWERKEY1 Register
05B2	**RTC_POWERKEY2**	16	RTC_POWERKEY2 Register
05B4	**RTC_PDN1**	16	PDN1
05B6	**RTC_PDN2**	16	PDN2
05B8	**RTC_SPAR0**	16	Spare Register for Specific Purpose 0
05BA	**RTC_SPAR1**	16	Spare Register for Specific Purpose 1
05BC	**RTC_PROT**	16	Lock/Unlock Scheme to Prevent RTC Miswriting
05BE	**RTC_DIFF**	16	**One-Time Calibration Offset** This register is fixed at 0 when RTC_POWERKEY1 and RTC_POWERKEY2 unmatch correct values.
05C0	**RTC_CALI**	16	**Repeat Calibration Offset** This register is fixed at 0 when RTC_POWERKEY1 and RTC_POWERKEY2 unmatch correct values.
05C2	**RTC_WRTGR**	16	**Enable Transfers from Core to RTC in Queue**
05C4	**RTC_CON**	16	**Other RTC Control Register** Note: GPU, GOE, LPRST, LPEN and GPEN are tie0 and F32KOB is tie1 internally when RTC_POWERKEY1 and RTC_POWERKEY2 do not match the correct values. After changing the RTC_CON, write WRTGR=1 to take

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
			effect.
0608	RTC_TC_SEC_SEC	16	Security RTC Seconds Time Counter Register
060A	RTC_TC_MIN_SEC	16	Security RTC Minutes Time Counter Register
060C	RTC_TC_HOU_SEC	16	Security RTC Hours Time Counter Register
060E	RTC_TC_DOM_SEC	16	Security RTC Day-of-Month Time Counter Register
0610	RTC_TC_DOW_SEC	16	Security RTC Day-of-Week Time Counter Register
0612	RTC_TC_MTH_SEC	16	Security RTC Month Time Counter Register
0614	RTC_TC_YEA_SEC	16	Security RTC Year Time Counter Register
0616	RTC_SEC_CK_PDN	16	Security RTC Clock Control Register
0618	RTC_SEC_WRTGR	16	Enable Transfers from Core to Security RTC in Queue
0788	DCXO_CW00	16	DCXO Code Word 0
078A	DCXO_CW00_SET	16	DCXO Code Word 0 Set
078C	DCXO_CW00_CLR	16	DCXO Code Word 0 Clear
078E	DCXO_CW01	16	DCXO Code Word 1
0790	DCXO_CW02	16	DCXO Code Word 2
0792	DCXO_CW03	16	DCXO Code Word 3
0794	DCXO_CW04	16	DCXO Code Word 4
0796	DCXO_CW05	16	DCXO Code Word 5
0798	DCXO_CW06	16	DCXO Code Word 6
079A	DCXO_CW07	16	DCXO Code Word 7
079C	DCXO_CW08	16	DCXO Code Word 8
079E	DCXO_CW09	16	DCXO Code Word 9
07A0	DCXO_CW10	16	DCXO Code Word 10
07A2	DCXO_CW11	16	DCXO Code Word 11
07A4	DCXO_CW11_SET	16	DCXO Code Word 11 Set
07A6	DCXO_CW11_CLR	16	DCXO Code Word 11 Clear
07A8	DCXO_CW12	16	DCXO Code Word 12
07AA	DCXO_CW13	16	DCXO Code Word 13
07AC	DCXO_CW14	16	DCXO Code Word 14
07AE	DCXO_CW15	16	DCXO Code Word 15
07B0	DCXO_CW16	16	DCXO Code Word 16
07B2	DCXO_CW17	16	DCXO Code Word 17
07B8	DCXO_CW20	16	DCXO Code Word 20
07BA	DCXO_CW21	16	DCXO Code Word 21
07BC	DCXO_CW22	16	DCXO Code Word 22
091A	PSC_TOP_INT_STATUS0	16	PSC_TOP INT Status Register 0
098A	STRUP_ANA_CON1	16	STRUP Control Register 1
0A08	PPCCTL0	16	PPC Control 0 Register
0A0E	PPCCFG0	16	PPC Configuration 0 Register
0A1C	STRUP_CON4	16	STRUP DIG Control Register N4
0A1E	STRUP_CON5	16	STRUP DIG Control Register N5
0A2C	STRUP_CON12	16	STRUP DIG Control Register 12
0A2E	STRUP_CON13	16	STRUP DIG Control Register 13
0A88	CHR_TOP_CON0	16	Charger Top Control Register 0
0A8C	CHR_TOP_CON2	16	Charger Top Control Register 2

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
0A8E	CHR_TOP_CON3	16	Charger Top Control Register 3
0A92	CHR_TOP_CON5	16	Charger Top Control Register 5
0A94	CHR_TOP_CON6	16	Charger Top Control Register 6
0B88	CHR_CON0	16	Charger Control Register 0
0B8A	CHR_CON1	16	Charger Control Register 1
0B8C	CHR_CON2	16	Charger Control Register 2
0B8E	CHR_CON3	16	Charger Control Register 3
0B94	CHR_CON6	16	Charger Control Register 6
0B98	CHR_CON8	16	Charger Control Register 8
0B9A	CHR_CON9	16	Charger Control Register 9
0D12	FGADC_CAR_CON0	16	FGADC_CAR Control Register 0
0D14	FGADC_CAR_CON1	16	FGADC_CAR Control Register 1
0D16	FGADC_CAR_CON2	16	FGADC_CAR Control Register 2
0D20	FGADC_NTER_CON0	16	FGADC_NTER Control Register 0
0D22	FGADC_NTER_CON1	16	FGADC_NTER Control Register 1
0D24	FGADC_NTER_CON2	16	FGADC_NTER Control Register 2
0D8A	FGADC_CUR_CON0	16	FGADC_CUR Control Register 0
0E08	BATON_ANA_CON0	16	BATON Analog Control Register 0
1088	AUXADC_ADC0	16	AUXADC ADC Register 0
108A	AUXADC_ADC1	16	AUXADC ADC Register 1
108C	AUXADC_ADC2	16	AUXADC ADC Register 2
108E	AUXADC_ADC3	16	AUXADC ADC Register 3
1090	AUXADC_ADC4	16	AUXADC ADC Register 4
1092	AUXADC_ADC5	16	AUXADC ADC Register 5
1094	AUXADC_ADC6	16	AUXADC ADC Register 6
1096	AUXADC_ADC7	16	AUXADC ADC Register 7
1098	AUXADC_ADC8	16	AUXADC ADC Register 8
109A	AUXADC_ADC9	16	AUXADC ADC Register 9
109C	AUXADC_ADC10	16	AUXADC ADC Register 10
109E	AUXADC_ADC11	16	AUXADC ADC Register 11
10A0	AUXADC_ADC12	16	AUXADC ADC Register 12
10A2	AUXADC_ADC14	16	AUXADC ADC Register 14
10A4	AUXADC_ADC16	16	AUXADC ADC Register 16
10A6	AUXADC_ADC17	16	AUXADC ADC Register 17
10A8	AUXADC_ADC18	16	AUXADC ADC Register 18
10AA	AUXADC_ADC19	16	AUXADC ADC Register 19
10AC	AUXADC_ADC20	16	AUXADC ADC Register 20
10AE	AUXADC_ADC21	16	AUXADC ADC Register 21
10B0	AUXADC_ADC22	16	AUXADC ADC Register 22
10B2	AUXADC_ADC23	16	AUXADC ADC Register 23
10B4	AUXADC_ADC24	16	AUXADC ADC Register 24
10B6	AUXADC_ADC25	16	AUXADC ADC Register 25
10B8	AUXADC_ADC26	16	AUXADC ADC Register 26

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
10BA	AUXADC_ADC27	16	AUXADC ADC Register 27
10BC	AUXADC_ADC29	16	AUXADC ADC Register 29
10BE	AUXADC_ADC30	16	AUXADC ADC Register 30
10C0	AUXADC_ADC31	16	AUXADC ADC Register 31
10C2	AUXADC_ADC32	16	AUXADC ADC Register 32
10C4	AUXADC_ADC33	16	AUXADC ADC Register 33
10C6	AUXADC_ADC34	16	AUXADC ADC Register 34
10C8	AUXADC_ADC35	16	AUXADC ADC Register 35
10CA	AUXADC_ADC36	16	AUXADC ADC Register 36
10D4	AUXADC_ADC42	16	AUXADC ADC Register 42
10D6	AUXADC_ADC43	16	AUXADC ADC Register 43
10D8	AUXADC_ADC46	16	AUXADC ADC Register 46
10DA	AUXADC_ADC47	16	AUXADC ADC Register 47
1108	AUXADC_STA0	16	AUXADC_STA0
110A	AUXADC_STA1	16	AUXADC_STA1
110C	AUXADC_STA2	16	AUXADC_STA2
140C	BUCK_TOP_CLK_CON0	16	BUCK_TOP Clock Control 0
1434	BUCK_TOP_OC_CON0	16	BUCK_TOP OC Control Register 0
1488	BUCK_VPROC_CON0	16	BUCK VPROC Control 0
148A	BUCK_VPROC_CON1	16	BUCK VPROC Control 1
14AA	BUCK_VPROC_ELR0	16	BUCK_VPROC ELR 0 Register
1508	BUCK_VCORE_CON0	16	BUCK VCORE Control 0
150A	BUCK_VCORE_CON1	16	BUCK VCORE Control 1
152A	BUCK_VCORE_ELR0	16	BUCK_VCORE ELR 0 Register
1588	BUCK_VMODEM_CON0	16	BUCK VMODEM Control 0
158A	BUCK_VMODEM_CON1	16	BUCK VMODEM Control 1
15AA	BUCK_VMODEM_ELR0	16	BUCK_VMODEM ELR 0 Register
1608	BUCK_VS1_CON0	16	BUCK VS1 Control 0
160A	BUCK_VS1_CON1	16	BUCK VS1 Control 1
1632	BUCK_VS1_ELR0	16	BUCK_VS1 ELR 0 Register
1688	BUCK_VPA_CON0	16	BUCK VPA Control 0
168A	BUCK_VPA_CON1	16	BUCK VPA Control 1
170A	SMPS_ANA_CON1	16	SMPS Control Register 1
170C	SMPS_ANA_CON2	16	SMPS Control Register 2
170E	VCORE_VPROC_ANA_CON0	16	VCORE_VPROC Control Register 0
1718	VCORE_VPROC_ANA_CON5	16	VCORE_VPROC Control Register 5
174C	SMPS_ELR_0	16	SMPS ELR 0 Register

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
188C	LDO_TOP_CLK_DCM_CON0	16	LDO DCM Control Register 0
188E	LDO_TOP_CLK_VIO28_CON0	16	LDO VIO28 Clock Gating Control Register 0
1890	LDO_TOP_CLK_VIO18_CON0	16	LDO VIO18 Clock Gating Control Register 0
1892	LDO_TOP_CLK_VAUD28_CON0	16	LDO VAUD28 Clock Gating Control Register 0
1894	LDO_TOP_CLK_VDRAM_CON0	16	LDO VDRAM Clock Gating Control Register 0
1896	LDO_TOP_CLK_VSRAM_PROC_CON0	16	LDO VSRAM_PROC Clock Gating Control Register 0
1898	LDO_TOP_CLK_VSRAM_OTHERS_CON0	16	LDO VSRAM_OTHERS Clock Gating Control Register 0
189A	LDO_TOP_CLK_VAUX18_CON0	16	LDO VAUX18 Clock Gating Control Register 0
189C	LDO_TOP_CLK_VUSB33_CON0	16	LDO VUSB33 Clock Gating Control Register 0
189E	LDO_TOP_CLK_VEMC_CON0	16	LDO VEMC Clock Gating Control Register 0
18A0	LDO_TOP_CLK_VXO22_CON0	16	LDO VXO22 Clock Gating Control Register 0
18A2	LDO_TOP_CLK_VSIM1_CON0	16	LDO VSIM1 Clock Gating Control Register 0
18A4	LDO_TOP_CLK_VSIM2_CON0	16	LDO VSIM2 Clock Gating Control Register 0
18A6	LDO_TOP_CLK_VCAMD_CON0	16	LDO VCAMD Clock Gating Control Register 0
18A8	LDO_TOP_CLK_VCAMIO_CON0	16	LDO VCAMIO Clock Gating Control Register 0
18AA	LDO_TOP_CLK_VEFUSE_CON0	16	LDO VEFUSE Clock Gating Control Register 0
18AC	LDO_TOP_CLK_VCN33_CON0	16	LDO VCN33 Clock Gating Control Register 0
18AE	LDO_TOP_CLK_VCN18_CON0	16	LDO VCN18 Clock Gating Control Register 0
18B0	LDO_TOP_CLK_VCN28_CON0	16	LDO VCN28 Clock Gating Control Register 0
18B2	LDO_TOP_CLK_VIBR_CON0	16	LDO VIBR Clock Gating Control Register 0
18B4	LDO_TOP_CLK_VFE28_CON0	16	LDO VFE28 Clock Gating Control Register 0
18B6	LDO_TOP_CLK_VMCH_CON0	16	LDO VMCH Clock Gating Control Register 0
18B8	LDO_TOP_CLK_VMC_CON0	16	LDO VMC Clock Gating Control Register 0
18BA	LDO_TOP_CLK_VRF18_CON0	16	LDO VRF18 Clock Gating Control Register 0
18BC	LDO_TOP_CLK_VLDO28_CON0	16	LDO VLDO28 Clock Gating Control Register 0
18BE	LDO_TOP_CLK_VRF12_CON0	16	LDO VRF12 Clock Gating Control Register 0
18C0	LDO_TOP_CLK_VCAMA_CON0	16	LDO VCAMA Clock Gating Control Register 0

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
18C2	LDO_TOP_CLK_TREF_CON0	16	LDO TREF Clock Gating Control Register 0
1916	LDO_VXO22_CON1	16	LDO VXO22 Control Register 1
192A	LDO_VAUX18_CON1	16	LDO VAUX18 Control Register 1
193E	LDO_VAUD28_CON1	16	LDO VAUD28 Control Register 1
1952	LDO_VIO28_CON1	16	LDO VIO28 Control Register 1
1966	LDO_VIO18_CON1	16	LDO VIO18 Control Register 1
197A	LDO_VDRAM_CON1	16	LDO VDRAM Control Register 1
1996	LDO_VEMC_CON1	16	LDO VEMC Control Register 1
19AC	LDO_VUSB33_CON1	16	LDO VUSB33 Control Register 1
19CE	LDO_VSRAM_PROC_DBG1	16	LDO VSRAM_PROC Debug 1
19EC	LDO_VSRAM_OTHERS_DBG1	16	LDO VSRAM_OTHERS Debug 1
1A08	LDO_VFE28_CON0	16	LDO VFE28 Control Register 0
1A0A	LDO_VFE28_OP_EN	16	LDO VFE28 Operation Enable
1A16	LDO_VFE28_CON1	16	LDO VFE28 Control Register 1
1A1C	LDO_VRF18_CON0	16	LDO VRF18 Control Register 0
1A1E	LDO_VRF18_OP_EN	16	LDO VRF18 Operation Enable
1A2A	LDO_VRF18_CON1	16	LDO VRF18 Control Register 1
1A30	LDO_VRF12_CON0	16	LDO VRF12 Control Register 0
1A32	LDO_VRF12_OP_EN	16	LDO VRF12 Operation Enable
1A3E	LDO_VRF12_CON1	16	LDO VRF12 Control Register 1
1A44	LDO_VEFUSE_CON0	16	LDO VEFUSE Control Register 0
1A46	LDO_VEFUSE_OP_EN	16	LDO VEFUSE Operation Enable
1A52	LDO_VEFUSE_CON1	16	LDO VEFUSE Control Register 1
1A58	LDO_VCN18_CON0	16	LDO VCN18 Control Register 0
1A5A	LDO_VCN18_OP_EN	16	LDO VCN18 Operation Enable
1A66	LDO_VCN18_CON1	16	LDO VCN18 Control Register 1
1A6C	LDO_VCAMA_CON0	16	LDO VCAMA Control Register 0
1A6E	LDO_VCAMA_OP_EN	16	LDO VCAMA Operation Enable
1A7A	LDO_VCAMA_CON1	16	LDO VCAMA Control Register 1
1A88	LDO_VCAMD_CON0	16	LDO VCAMD Control Register 0
1A8A	LDO_VCAMD_OP_EN	16	LDO VCAMD Operation Enable
1A96	LDO_VCAMD_CON1	16	LDO VCAMD Control Register 1
1A9C	LDO_VCAMIO_CON	16	LDO VCAMIO Control Register 0

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
	0		
1A9E	LDO_VCAMIO_OP_EN	16	LDO VCAMIO Operation Enable
1AAA	LDO_VCAMIO_CON1	16	LDO VCAMIO Control Register 1
1AB0	LDO_VMC_CON0	16	LDO VMC Control Register 0
1AB2	LDO_VMC_OP_EN	16	LDO VMC Operation Enable
1ABE	LDO_VMC_CON1	16	LDO VMC Control Register 1
1AC4	LDO_VMCH_CON0	16	LDO VMCH Control Register 0
1AC6	LDO_VMCH_OP_EN	16	LDO VMCH Operation Enable
1AD2	LDO_VMCH_CON1	16	LDO VMCH Control Register 1
1AD8	LDO_VSIM1_CON0	16	LDO VSIM1 Control Register 0
1ADA	LDO_VSIM1_OP_EN	16	LDO VSIM1 Operation Enable
1AE6	LDO_VSIM1_CON1	16	LDO VSIM1 Control Register 1
1AEC	LDO_VSIM2_CON0	16	LDO VSIM2 Control Register 0
1AEE	LDO_VSIM2_OP_EN	16	LDO VSIM2 Operation Enable
1AFA	LDO_VSIM2_CON1	16	LDO VSIM2 Control Register 1
1B08	LDO_VIBR_CON0	16	LDO VIBR Control Register 0
1B0A	LDO_VIBR_OP_EN	16	LDO VIBR Operation Enable
1B16	LDO_VIBR_CON1	16	LDO VIBR Control Register 1
1B1C	LDO_VCN33_CON0_0	16	LDO VCN33 bt Control Register 0
1B1E	LDO_VCN33_OP_EN	16	LDO VCN33 Operation Enable
1B2A	LDO_VCN33_CON0_1	16	LDO VCN33 wifi Control Register 0
1B2C	LDO_VCN33_CON1	16	LDO VCN33 Control Register 1
1B32	LDO_VLDO28_CON0_0	16	LDO VLDO28 AF Control Register 0
1B34	LDO_VLDO28_OP_EN	16	LDO VLDO28 Operation Enable
1B40	LDO_VLDO28_CON0_1	16	LDO VLDO28 TP Control Register 0
1B42	LDO_VLDO28_CON1	16	LDO VLDO28 Control Register 1
1B88	LDO_VCN28_CON0	16	LDO VCN28 Control Register 0
1B8A	LDO_VCN28_OP_EN	16	LDO VCN28 Operation Enable
1B96	LDO_VCN28_CON1	16	LDO VCN28 Control Register 1
1B9C	VRTC_CON0	16	VRTC Control Register 0
1B9E	LDO_TREF_CON0	16	LDO TREF Control Register 0
1BA0	LDO_TREF_OP_EN	16	LDO TREF Operation Enable
1BAC	LDO_TREF_CON1	16	LDO TREF Control Register 1
1C08	VFE28_ANA_CON0	16	VFE28 Control Register 0
1C0C	VCN28_ANA_CON0	16	VCN28 Control Register 0
1C1C	VCN33_ANA_CON0	16	VCN33 Control Register 0
1C24	VLDO28_ANA_CON	16	VLDO28 Control Register 0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
	0		
1C2C	VIBR_ANA_CON0	16	VIBR Control Register 0
1C30	VSIM1_ANA_CON0	16	VSIM1 Control Register 0
1C34	VSIM2_ANA_CON0	16	VSIM2 Control Register 0
1C38	VMCH_ANA_CON0	16	VMCH Control Register 0
1C3C	VMC_ANA_CON0	16	VMC Control Register 0
1C40	VCAMIO_ANA_CON0	16	VCAMIO Control Register 0
1C44	VCN18_ANA_CON0	16	VCN18 Control Register 0
1C48	VRF18_ANA_CON0	16	VRF18 Control Register 0
1C52	VRF12_ANA_CON0	16	VRF12 Control Register 0
1C8C	VCAMA_ANA_CON0	16	VCAMA Control Register 0
1C90	VEFUSE_ANA_CON0	16	VEFUSE Control Register 0
1C94	VCAMD_ANA_CON0	16	VCAMD Control Register 0
1E10	XPP_TOP_CKPDN_CON0	16	XPP_TOP_CKPDN Control Register 0
1E12	XPP_TOP_CKPDN_CON0_SET	16	XPP_TOP_CKPDN_CON0 Register SET
1E14	XPP_TOP_CKPDN_CON0_CLR	16	XPP_TOP_CKPDN_CON0 Register CLR
1E16	XPP_TOP_CKSEL_CON0	16	XPP_TOP_CKSEL Control Register 0
1E18	XPP_TOP_CKSEL_CON0_SET	16	XPP_TOP_CKSEL_CON0 Register SET
1E1A	XPP_TOP_CKSEL_CON0_CLR	16	XPP_TOP_CKSEL_CON0 Register CLR
1E88	ISINK1_CON0	16	ISINK1 Control Register 0
1E8A	ISINK1_CON1	16	ISINK1 Control Register 1
1E8C	ISINK1_CON2	16	ISINK1 Control Register 2
1E8E	ISINK1_CON3	16	ISINK1 Control Register 3
1E94	ISINK_SFSTR	16	ISINK Soft Start
1E96	ISINK_EN_CTRL	16	ISINK Enable Control
1E98	ISINK_MODE_CTRL	16	ISINK Mode Control
1E9A	DRIVER_ANA_CON0	16	DRIVER Control Register 0
1E9C	ISINK_ANA_CON0	16	ISINK Read-Only Register 0
1F08	CHRIND_CON0	16	CHRIND Control Register 0
1F0A	CHRIND_CON1	16	CHRIND Control Register 1
1F0C	CHRIND_CON2	16	CHRIND Control Register 2
1F0E	CHRIND_CON3	16	CHRIND Control Register 3
1F10	CHRIND_CON4	16	CHRIND Control Register 4
1F12	CHRIND_EN_CTRL	16	CHRIND Enable Control Simple
208C	AUD_TOP_CKPDN_CON0	16	AUDIO CLK Power Down Register 0
2092	AUD_TOP_CKSEL_CON0	16	AUDIO CKSEL Control Register 0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
20B4	AUDNCP_CLKDIV_CON0	16	AUDNCP_CLKDIV Control Register 0
20B6	AUDNCP_CLKDIV_CON1	16	AUDNCP_CLKDIV Control Register 1
20B8	AUDNCP_CLKDIV_CON2	16	AUDNCP_CLKDIV Control Register 2
20BA	AUDNCP_CLKDIV_CON3	16	AUDNCP_CLKDIV Control Register 3
20BC	AUDNCP_CLKDIV_CON4	16	AUDNCP_CLKDIV Control Register 4
20BE	AUD_TOP_MON_CON0	16	AUD_TOP_MON control register 0
2108	AFE_UL_DL_CON0	16	Audio UL and DL Control Register 0
210A	AFE_DL_SRC2_CON0_L	16	AFE_DL_SRC2 Control Register 0 Low Part
210C	AFE_UL_SRC_CON0_H	16	AFE uplink SRC Control Register 0 High Part
210E	AFE_UL_SRC_CON0_L	16	AFE uplink SRC Control Register 0 Low Part
2110	AFE_TOP_CON0	16	AFE top Control Register 0
2112	AUDIO_TOP_CON0	16	AUDIO top Control Register 0
2114	AFE_MON_DEBUG0	16	AFE Monitor Output Debug Register 0
2116	AFUNC_AUD_CON0	16	A_FUNC AUDIO Control Register 0
2118	AFUNC_AUD_CON1	16	A_FUNC AUDIO Control Register 1
211A	AFUNC_AUD_CON2	16	A_FUNC AUDIO Control Register 2
211C	AFUNC_AUD_CON3	16	A_FUNC AUDIO Control Register 3
211E	AFUNC_AUD_CON4	16	A_FUNC AUDIO Control Register 4
2120	AFUNC_AUD_CON5	16	A_FUNC AUDIO Control Register 5
2122	AFUNC_AUD_CON6	16	A_FUNC AUDIO Control Register 6
2124	AFUNC_AUD_MON0	16	A_FUNC AUDIO Monitor Register 0
2126	AUDRC_TUNE_MON0	16	Analog Monitor Register 0
2140	AFE_SGEN_CFG0	16	AFE SGEN CON0
2142	AFE_SGEN_CFG1	16	**AFE SGEN CON1** Sets up SGEN tone freq.
2144	AFE_ADC_ASYNC_FIFO_CFG	16	AFE_ADC_SYNC_FIFO_CFG
2146	AFE_DCCLK_CFG0	16	AFE_DCCLK_CFG0
2148	AFE_DCCLK_CFG1	16	AFE_DCCLK_CFG1
2188	AUDENC_ANA_CON0	16	AUDENC Control Register 0
218A	AUDENC_ANA_CON1	16	AUDENC Control Register 1
218C	AUDENC_ANA_CON2	16	AUDENC Control Register 2
218E	AUDENC_ANA_CON3	16	AUDENC Control Register 3
2190	AUDENC_ANA_CON4	16	AUDENC Control Register 4

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
2192	AUDENC_ANA_CON5	16	AUDENC Control Register 5
2194	AUDENC_ANA_CON6	16	AUDENC Control Register 6
2196	AUDENC_ANA_CON7	16	AUDENC Control Register 7
2198	AUDENC_ANA_CON8	16	AUDENC Control Register 8
219A	AUDENC_ANA_CON9	16	AUDENC Control Register 9
219C	AUDENC_ANA_CON10	16	AUDENC Control Register 10
219E	AUDENC_ANA_CON11	16	AUDENC Control Register 11
2208	AUDDEC_ANA_CON0	16	AUDDEC Control Register 0
220A	AUDDEC_ANA_CON1	16	AUDDEC Control Register 1
220C	AUDDEC_ANA_CON2	16	AUDDEC Control Register 2
220E	AUDDEC_ANA_CON3	16	AUDDEC Control Register 3
2210	AUDDEC_ANA_CON4	16	AUDDEC Control Register 4
2212	AUDDEC_ANA_CON5	16	AUDDEC Control Register 5
2214	AUDDEC_ANA_CON6	16	AUDDEC Control Register 6
2216	AUDDEC_ANA_CON7	16	AUDDEC Control Register 7
2218	AUDDEC_ANA_CON8	16	AUDDEC Control Register 8
221A	AUDDEC_ANA_CON9	16	AUDDEC Control Register 9
221C	AUDDEC_ANA_CON10	16	AUDDEC Control Register 10
221E	AUDDEC_ANA_CON11	16	AUDDEC Control Register 11
2220	AUDDEC_ANA_CON12	16	AUDDEC Control Register 12
2222	AUDDEC_ANA_CON13	16	AUDDEC Control Register 13
2226	AUDDEC_ELR_0	16	AUDDEC ELR 0 Register
2288	ZCD_CON0	16	ZCD Control Register 0
228A	ZCD_CON1	16	ZCD Control Register 1
228C	ZCD_CON2	16	ZCD Control Register 2
228E	ZCD_CON3	16	ZCD Control Register 3
2290	ZCD_CON4	16	ZCD Control Register 4
2292	ZCD_CON5	16	ZCD Control Register 5
2308	ACCDET_CON0	16	ACCDET Control Register 0
230A	ACCDET_CON1	16	ACCDET Control Register 1
230C	ACCDET_CON2	16	ACCDET Control Register 2
230E	ACCDET_CON3	16	ACCDET Control Register 3

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Address	Name	Width	Register Function
2310	ACCDET_CON4	16	ACCDET Control Register 4
2312	ACCDET_CON5	16	ACCDET Control Register 5
2314	ACCDET_CON6	16	ACCDET Control Register 6
2316	ACCDET_CON7	16	ACCDET Control Register 7
2318	ACCDET_CON8	16	ACCDET Control Register 8
231A	ACCDET_CON9	16	ACCDET Control Register 9
231C	ACCDET_CON10	16	ACCDET Control Register 10
2320	ACCDET_CON12	16	ACCDET Control Register 12
2324	ACCDET_CON14	16	ACCDET Control Register 14
2326	ACCDET_CON15	16	ACCDET Control Register 15
2328	ACCDET_CON16	16	ACCDET Control Register 16
232C	ACCDET_CON18	16	ACCDET Control Register 18
2332	ACCDET_CON21	16	ACCDET Control Register 21
233A	ACCDET_CON25	16	ACCDET Control Register 25
233C	ACCDET_CON26	16	ACCDET Control Register 26
233E	ACCDET_CON27	16	ACCDET Control Register 27

000C PONSTS Power On Source Record Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												STS_RBOOT	STS_SPAR	STS_CHRIN	STS_RTCA	STS_PWRKEY
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	STS_RBOOT	Power on for cold reset
3	STS_SPAR	Power on for SPAR event
2	STS_CHRIN	Power on for charger insertion
1	STS_RTCA	Power on for RTC alarm
0	STS_PWRKEY	Power on for PWREKY press

000E POFFSTS Power Off Source Record Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					STS_PUPSRC	STS_WDT	STS_DDLO	STS_BWDT	STS_NORMOFF	STS_PKEYLP	STS_CRST	STS_WRST	STS_THRDN	STS_PSOC	STS_PGFAIL	STS_UVLO
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	STS_PUPSRC	Power off for power source missing

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
10	STS_WDT	AP WDT
9	STS_DDLO	DDLO occurred after system on
8	STS_BWDT	Power off for BWDT
7	STS_NORMOFF	Power off for PWRHOLD clear
6	STS_PKEYLP	Power off for power key(s) long press
5	STS_CRST	Power off for cold reset
4	STS_WRST	Power reset for warm reset
3	STS_THRDN	Power off for thermal shutdown
2	STS_PSOC	Power off for default on BUCK OC
1	STS_PGFAIL	Power off for PWRGOOD failure
0	STS_UVLO	Power off for UVLO event

0010 **PSTSCTL** **Power On/Off Status Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_PONSTS_CLR								RG_POFFSTS_CLR
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
8	RG_PONSTS_CLR	Clears PONSTS
0	RG_POFFSTS_CLR	Clears POFFSTST and PG/OC status

0014 **PG_SDN_STS0** **Power Good Shutdown Status 0** **FFFE**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VS1_PG_STATUS	STRUP_VCORE_PG_STATUS	STRUP_VMODEM_PG_STATUS	STRUP_VPROC_PG_STATUS	STRUP_VXO22_PG_STATUS	STRUP_VAUX18_PG_STATUS	STRUP_VSRAM_OTHERS_PG_STATUS	STRUP_VSRAM_PROC_PG_STATUS	STRUP_VIO18_PG_STATUS	STRUP_VEMC_PG_STATUS	STRUP_VIO28_PG_STATUS	STRUP_VDRAM_PG_STATUS	STRUP_VUSB33_PG_STATUS	STRUP_VAUD28_PG_STATUS	STRUP_EXT_PMIC_PG_STATUS	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit(s)	Name	Description
15	STRUP_VS1_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
14	STRUP_VCORE_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: Power good
13	STRUP_VMODEM_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
12	STRUP_VPROC_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
11	STRUP_VXO22_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
10	STRUP_VAUX18_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
9	STRUP_VSRAM_OTHERS_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
8	STRUP_VSRAM_PROC_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
7	STRUP_VIO18_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
6	STRUP_VEMC_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
5	STRUP_VIO28_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
4	STRUP_VDRAM_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
3	STRUP_VUSB33_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
2	STRUP_VAUD28_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good
1	STRUP_EXT_PMIC_PG_STATUS	**Shut down PG status (cleared by SW)** 0: Power not good 1: Power good

0016 **OC_SDN_STS0** **OC Shutdown Status 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VS1_OC_STATUS	STRUP_VCORE_OC_STATUS	STRUP_VMODEM_OC_STATUS	STRUP_VPROC_OC_STATUS												

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	STRUP_VS1_OC_STATUS	**Shut down OC status (cleared by SW)** 0: No OC 1: OC occurs.
14	STRUP_VCORE_OC_STATUS	**Shut down OC status (cleared by SW)** 0: No OC 1: OC occurs.
13	STRUP_VMODEM_OC_STATUS	**Shut down OC status (cleared by SW)** 0: No OC 1: OC occurs.
12	STRUP_VPROC_OC_STATUS	**Shut down OC status (cleared by SW)** 0: No OC 1: OC occurs.

014C TOP_RST_MISC Reset Control Misc 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_PWRKEY_RST_TD								RG_WDTRSTB_DEB					RG_WDTRSTB_EN
Type			RW								RW					RW
Reset			0	0							0					0

Bit(s)	Name	Description
13:12	RG_PWRKEY_RST_TD	**Long pressed time to issue reset** 2'b00: 8 sec 2'b01: 11 sec 2'b10: 14 sec 2'b11: 5 sec
5	RG_WDTRSTB_DEB	**Enables WDTRSTB debounce** 1'b0: No debounce 1'b1: Add debounce 1.6ms
0	RG_WDTRSTB_EN	**WDTRSTB (external watchdog) reset from AP** 1'b0: Disable 1'b1: Enable

019E TOP_INT_STATUS0 TOP_INT_STATUS Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								INT_STATUS_MISC_TOP	INT_STATUS_AUD_TOP	INT_STATUS_XPP_TOP	INT_STATUS_HK_TOP	INT_STATUS_BM_TOP	INT_STATUS_SCK_TOP	INT_STATUS_PSC_TOP	INT_STATUS_LDO_TOP	INT_STATUS_BUCK_TOP
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	INT_STATUS_MISC_TOP	**Interrupt mask for TOP** 0: Unmask interrupt 1: Mask interrupt
7	INT_STATUS_AUD_TOP	**Interrupt mask for AUD** 0: Unmask interrupt 1: Mask interrupt
6	INT_STATUS_XPP_TOP	**Interrupt mask for XPP** 0: Unmask interrupt 1: Mask interrupt
5	INT_STATUS_HK_TOP	**Interrupt mask for HK** 0: Unmask interrupt 1: Mask interrupt
4	INT_STATUS_BM_TOP	**Interrupt mask for BM** 0: Unmask interrupt 1: Mask interrupt
3	INT_STATUS_SCK_TOP	**Interrupt mask for SCK** 0: Unmask interrupt 1: Mask interrupt
2	INT_STATUS_PSC_TOP	**Interrupt mask for PSC** 0: Unmask interrupt 1: Mask interrupt
1	INT_STATUS_LDO_TOP	**Interrupt mask for LDO** 0: Unmask interrupt 1: Mask interrupt
0	INT_STATUS_BUCK_TOP	**Sets up TOP_INTM_CON0** 0: Unmask interrupt 1: Mask interrupt

038E **TOP_CLK_TRIM** **TOP_CLK_TRIM Register** **00C0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_OSC_128K_TRIM														
Type		RO														
Reset		0	0	0	0	0	0									

Bit(s)	Name	Description
14:9	DA_OSC_128K_TRIM	128kHz OSC trimming bit

0390 **OTP_CON0** **OTP Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_OTP_PA							
Type									RW							
Reset									0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
7:0	RG_OTP_PA	OTP PA

0392 OTP_CON1 OTP Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_OTP_PDIN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_OTP_PDIN	OTP PDIN

0394 OTP_CON2 OTP Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PTM	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PTM	OTP PTM

0396 OTP_CON3 OTP Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PWE	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PWE	OTP PWE

0398 OTP_CON4 OTP Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_PPROG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PPROG	OTP PPROG

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

039A **OTP_CON5** **OTP Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_OTP_PWE_SRC**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PWE_SRC	**Selects OTP write (fusing) PWE source** 0: From IO pad 1: From register

039C **OTP_CON6** **OTP Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_PROG_PKEY**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_PROG_PKEY	OTP write (fusing) match key

039E **OTP_CON7** **OTP Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_RD_PKEY**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_RD_PKEY	OTP read match key

03A0 **OTP_CON8** **OTP Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_OTP_RD_TRIG**
Type																RW
Reset																0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_OTP_RD_TRIG	OTP SW read trigger

03A2 OTP_CON9 OTP Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_RD_RDY_BYPASS
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_RD_RDY_BYPASS	**Bypasses OTP read ready delay** 0: Not bypass 1: Bypass

03A4 OTP_CON10 OTP Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_SKIP_OTP_OUT
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_SKIP_OTP_OUT	**Skips reading from EFUSE macro** 0: Not skip 1: Skip

03A6 OTP_CON11 OTP Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_RD_SW
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_SW	**SW trigger read mode** 0: Non SW trigger read mode 1: SW trigger read mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

03A8 OTP_CON12 OTP Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_SW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_SW	Current SW trigger read value

03AA OTP_CON13 OTP Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_OTP_RD_ACK		RG_OTP_RD_BUSY
Type														RO		RO
Reset														0		0

Bit(s)	Name	Description
2	RG_OTP_RD_ACK	OTP read ack
0	RG_OTP_RD_BUSY	OTP busy status

03AC OTP_CON14 OTP Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_OTP_PA_SW						
Type										RO						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_OTP_PA_SW	Current SW trigger read row

0514 SCK_TOP_CKPDN_CON0 SCK_CKPDN Control Register 0 004B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_RTC_2SEC_OFF_DET_PDN	RG_RTC_26M_CK_PDN	RG_RTC_32K_CK_PDN	RG_RTC_MCLK_PDN	RG_RTC_SEC_32K_CK_PDN	RG_RTC_EOSC32_CK_PDN	RG_EOSC_CALI_TEST_CK_PDN	RG_RTC_SEC_MCLK_PDN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	1	0	0	1	0	1	1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
7	RG_RTC_2SEC_OFF_DET_PDN	**Powers down RTC_2SEC_OFF_DET** 0: Power on 1: Power down
6	RG_RTC_26M_CK_PDN	**Powers down RTC_26M_CK** 0: Power on 1: Power down
5	RG_RTC_32K_CK_PDN	**Powers down RTC_32K_CK** 0: Power on 1: Power down
4	RG_RTC_MCLK_PDN	**Powers down RTC_MCLK** 0: Power on 1: Power down
3	RG_RTC_SEC_32K_CK_PDN	**Powers down RTC_SEC_32K_CK** 0: Power on 1: Power down
2	RG_RTC_EOSC32_CK_PDN	**Powers down RTC_EOSC32_CK** 0: Power on 1: Power down
1	RG_EOSC_CALI_TEST_CK_PDN	**Powers down EOSC_CALI_TEST_CK** 0: Power on 1: Power down
0	RG_RTC_SEC_MCLK_PDN	**Powers down RTC_SEC_MCLK** 0: Power on 1: Power down

0516 **SCK_TOP_CKPDN_CON0_SET** **SCK_CKPDN Control Register 0 SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCK_TOP_CKPDN_CON0_SET							
Type									W1							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCK_TOP_CKPDN_CON0_SET	**Sets up SCK_TOP_CKPDN_CON0** 1'b0: Not set 1'b1: Set

0518 **SCK_TOP_CKPDN_CON0_CLR** **SCK_CKPDN Control Register 0 CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCK_TOP_CKPDN_CON0_CLR							
Type									W1							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
7:0	SCK_TOP_CKPDN_CON0_CLR	**Clears SCK_TOP_CKPDN_CON0** 1'b0: Not clear 1'b1: Clear

051A	SCK_TOP_CKHWEN_CON0	SCK_CKHWEN Control Register 0	03F1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_RTC_CLK_PDN_HWEN_RSV_0						RG_RTC_CLK_PDN_HWEN_RSV_1						RG_RTC_SEC_MCLK_PDN_HWEN	RG_RTC_SEC_32K_CK_PDN_HWEN	RG_RTC_MCLK_PDN_HWEN	RG_RTC_26M_CK_PDN_HWEN
Type	RW						RW						RW	RW	RW	RW
Reset	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1

Bit(s)	Name	Description
15:10	RG_RTC_CLK_PDN_HWEN_RSV_0	**RESERVED_0** 0: SW mode 1: HW mode
9:4	RG_RTC_CLK_PDN_HWEN_RSV_1	**RESERVED_1** 0: SW mode 1: HW mode
3	RG_RTC_SEC_MCLK_PDN_HWEN	**RTC_SEC_MCLK power down control** 0: SW mode 1: HW mode
2	RG_RTC_SEC_32K_CK_PDN_HWEN	**RTC_SEC_32K_CK power down control** 0: SW mode 1: HW mode
1	RG_RTC_MCLK_PDN_HWEN	**RTC_MCLK power down control** 0: SW mode 1: HW mode
0	RG_RTC_26M_CK_PDN_HWEN	**RTC_26M_CK power down control** 0: SW mode 1: HW mode

051C	SCK_TOP_CKHWEN_CON0_SET	SCK_CKHWEN_CON Register 0 SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_TOP_CKHWEN_CON_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:0	SCK_TOP_CKHWEN_CON_SET	**Sets up SCK_CKHWEN_CON** 1'b0: Not set 1'b1: Set

051E **SCK_TOP_CKHWEN_CON0_CLR** **SCK_CKHWEN_CON Register 0 CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_TOP_CKHWEN_CON_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SCK_TOP_CKHWEN_CON_CLR	**Clears SCK_CKHWEN_CON** 1'b0: Not clear 1'b1: Clear

0528 **SCK_TOP_INT_CON0** **SCK_TOP INT Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_INT_EN_RTC
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_INT_EN_RTC	**Enables RTC interrupt** 0: Not issue interrupt 1: Issue interrupt

052E **SCK_TOP_INT_MASK_CON0** **SCK_TOP INT mask Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_INT_MASK_RTC
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_INT_MASK_RT	**Masks RTC interrupt status**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	C	1'b0: Unmask interrupt status 1'b1: Mask interrupt status

0534 **SCK_TOP_INT_STATUS0** **SCK_TOP INT Status Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_INT_STATUS_RTC
Type																W1C
Reset																0

Bit(s)	Name	Description
0	RG_INT_STATUS_RTC	**RTC interrupt status** 0: No interrupt issued 1: Interrupt issued

0538 **SCK_TOP_INT_MISC_CON** **SCK_TOP INT MISC Control Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SCK_TOP_POLARITY
Type																RW
Reset																0

Bit(s)	Name	Description
0	SCK_TOP_POLARITY	**Inverts interrupt source polarity** 0: Not invert interrupt source 1: Invert interrupt source

0588 **RTC_BBPU** **Baseband Power Up** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY_BBPU									CBUSY	RELOAD	CLRPKY	AUTO	BBPU_INIT	BBPU_CLR	PWREN
Type	WO									RO	WO	WO	RW	WO	RW	RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:8	KEY_BBPU	**A bus write is acceptable only when KEY_BBPU=0x43.**
6	CBUSY	**The read/write channels between RTC/Core is busy.** This bit indicates high after software program sequence to anyone of RTC data registers and enable the transfer by RTC_WRTGR=1. By the way, it is high after the reset from low to high because RTC reloads the process.
5	RELOAD	**Reloads the values from RTC domain to Core domain** RTC will reload to synchronize the data from RTC to core when reset from 0 to 1. This bit can be treated as a debug bit.
4	CLRPKY	**Clears powerkey 1 and powerkey 2 at the same time** In some cases, software may clear powerkey 1 and powerkey 2. The BBWAKEUP depends on the matching specific patterns of powerkey 1 and powerkey 2. If any one of powerkey 1 or powerkey 2 or BBPU is cleared, BBWAKEUP will go low immediately. Software cannot program other control bits without power. By programming RTC_BBPU with CLRPKY=1 and BBPU=0 condition, RTC can clear powerkey 1, powerkey 2 and BBPU at the same moment.
3	AUTO	**Clears SPAR wvent in old legacy mode when SYSRST# transitions from high to low** 0: BBWAKEUP will not automatically be in the low state when SYSRST# transitions from high to low. 1: BBWAKEUP will be automatically in the low state when SYSRST# transitions from high to low. The function is only active when RTC_POWERKEY1 and RTC_POWERKEY2 match correct values.
2	BBPU_INIT	**Set this bit to 1'b1 to activate RTC to initialize SPAR and ALARM default status; otherwise SPAR and ALARM default value will be unknown. When the initialization is finished, this bit will be set to 1'b0 automatically by RTC HW.** 1'b1: Trigger RTC to initialize SPAR and ALRAM status
1	BBPU_CLR	**Set this bit to 1'b1 to clear SPAR and ALARM status to 1'b0.** This bit will automatically be set to 1'b0 when SPAR or ALRAM happens. 1'b1: Clear SPAR/ALRAM
0	PWREN	**Enables ALARM to wake up the system** 0: RTC alarm has no action on power switch. 1: When an RTC alarm occurs, alarm start-up will be set to 1 and the system powered on by RTC alarm wakeup.

058A **RTC_IRQ_STA** **RTC IRQ Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													LPSTA		TCSTA	ALSTA
Type													RO		RO	RO
Reset													0		0	0

Bit(s)	Name	Description
3	LPSTA	**Indicates IRQ status and whether or not LPD is asserted** 0: No IRQ occurs. The 32K clock is good. 1: IRQ occurs. The 32K clock is stopped or stops. This can be masked by LP_EN or cleared by initializing LPD.
1	TCSTA	**Indicates IRQ status and whether or not the tick condition has been met** 0: No IRQ occurs. The tick condition has not been met.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: IRQ occurs. The tick condition has been met.
0	ALSTA	**Indicates IRQ status and whether or not the alarm condition has been met** 0: No IRQ occurs. The alarm condition has not been met. 1: IRQ occurs. The alarm condition has been met.

058C **RTC_IRQ_EN** **RTC IRQ Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**LP_EN**	**ONESHOT**	**TC_EN**	**AL_EN**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	LP_EN	**Enables the control bit for IRQ generation if low power is detected (32k clock off)** 0: Disable IRQ generations 1: Enable LPD
2	ONESHOT	**Controls automatic reset of AL_EN and TC_EN.**
1	TC_EN	**Enables the control bit for IRQ generation if the tick condition has been met** 0: Disable IRQ generations 1: Enable the tick time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.
0	AL_EN	**Enables the control bit for IRQ generation if the alarm condition has been met** 0: Disable IRQ generations 1: Enable the alarm time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

058E **RTC_CII_EN** **Counter Increment IRQ Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**SECCII_1_8**	**SECCII_1_4**	**SECCII_1_2**	**YEACII**	**MTHCII**	**DOWCII**	**DOMCII**	**HOUCII**	**MINCII**	**SECCII**
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	SECCII_1_8	Set the bit to 1 to activate the IRQ at each one-eighth of a second update.
8	SECCII_1_4	Set the bit to 1 to activate the IRQ at each one-fourth of a second update.
7	SECCII_1_2	Set the bit to 1 to activate the IRQ at each one-half of a second update.
6	YEACII	Set the bit to 1 to activate the IRQ at each year update.
5	MTHCII	Set the bit to 1 to activate the IRQ at each month update.
4	DOWCII	Set the bit to 1 to activate the IRQ at each day-of-week update.
3	DOMCII	Set the bit to 1 to activate the IRQ at each day-of-month update.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
2	HOUCII	Set the bit to 1 to activate the IRQ at each hour update.
1	MINCII	Set the bit to 1 to activate the IRQ at each minute update.
0	SECCII	Set this bit to 1 to activate the IRQ at each second update.

0590 **RTC_AL_MASK** **RTC Alarm Mask** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										YEA_MSK	MTH_MSK	DOW_MSK	DOM_MSK	HOU_MSK	MIN_MSK	SEC_MSK
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	YEA_MSK	0: Condition (RTC_TC_YEA = RTC_AL_YEA) is checked to generate the alarm signal. 1: Condition (RTC_TC_YEA = RTC_AL_YEA) is masked, i.e. the value of RTC_TC_YEA does not affect the alarm IRQ generation.
5	MTH_MSK	0: Condition (RTC_TC_MTH = RTC_AL_MTH) is checked to generate the alarm signal. 1: Condition (RTC_TC_MTH = RTC_AL_MTH) is masked, i.e. the value of RTC_TC_MTH does not affect the alarm IRQ generation.
4	DOW_MSK	0: Condition (RTC_TC_DOW = RTC_AL_DOW) is checked to generate the alarm signal. 1: Condition (RTC_TC_DOW = RTC_AL_DOW) is masked, i.e. the value of RTC_TC_DOW does not affect the alarm IRQ generation.
3	DOM_MSK	0: Condition (RTC_TC_DOM = RTC_AL_DOM) is checked to generate the alarm signal. 1: Condition (RTC_TC_DOM = RTC_AL_DOM) is masked, i.e. the value of RTC_TC_DOM does not affect the alarm IRQ generation.
2	HOU_MSK	0: Condition (RTC_TC_HOU = RTC_AL_HOU) is checked to generate the alarm signal. 1: Condition (RTC_TC_HOU = RTC_AL_HOU) is masked, i.e. the value of RTC_TC_HOU does not affect the alarm IRQ generation.
1	MIN_MSK	0: Condition (RTC_TC_MIN = RTC_AL_MIN) is checked to generate the alarm signal. 1: Condition (RTC_TC_MIN = RTC_AL_MIN) is masked, i.e. the value of RTC_TC_MIN does not affect the alarm IRQ generation.
0	SEC_MSK	0: Condition (RTC_TC_SEC = RTC_AL_SEC) is checked to generate the alarm signal. 1: Condition (RTC_TC_SEC = RTC_AL_SEC) is masked, i.e. the value of RTC_TC_SEC does not affect the alarm IRQ generation.

0592 **RTC_TC_SEC** **RTC Seconds Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_SECOND					
Type											RW					
Reset											0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
5:0	TC_SECOND	**The second initial value for the time counter** Value range: 0~59

0594 **RTC_TC_MIN** **RTC Minutes Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_MINUTE					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_MINUTE	**The minute initial value for the time counter** Value range: 0~59

0596 **RTC_TC_HOU** **RTC Hours Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_HOUR				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_HOUR	**The hour initial value for the time counter** Value range: 0~23

0598 **RTC_TC_DOM** **RTC Day-of-Month Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_DOM				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_DOM	**The day-of-month initial value for the time counter** The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are 0.

059A **RTC_TC_DOW** **RTC Day-of-Week Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TC_DOW		
Type														RW		
Reset														0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
2:0	TC_DOW	**The day-of-week initial value for the time counter** Value range: 1~7

059C **RTC_TC_MTH** **RTC Month Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TC_MONTH			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TC_MONTH	**The month initial value for the time counter** Value range: 1~12

059E **RTC_TC_YEA** **RTC Year Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TC_YEAR						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	TC_YEAR	**The year initial value for the time counter** Value range: 0-~27 (2000~2127) Software can bias the year as multiples of 4 for the internal leap-year formula, e.g. 2000~2127, 1972~2099, 1904~2031. To simplify, RTC hardware treats all 4-multiple as leap years. If the range you define includes non-leap 4-multiple year (e.g. 2100), adjust to correct date by yourself (e.g. change Feb. 29th, 2100 to Mar. 1st, 2100). It is suggested to bias the range large than 1900 and less than 2100 to evade the manual adjusting, i.e. the bias values are suggested to be in the range of [-28,-96], that are (1972~2099) ~ (1904~ 031). Formal leap formula: if year modulo 400 is 0 then leap else if year modulo 100 is 0 then no_leap else if year modulo 4 is 0 then leap else no_leap

05A0 **RTC_AL_SEC** **RTC Second Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	K_EOSC32_VTCXO_ON_	RTC_LPD_OPT		BBPU_2SEC_STAT_STA	BBPU_2SEC_STAT_CLE	BBPU_2SEC_MODE		BBPU_2SEC_EN	BBPU_2SEC_CK_SEL	BBPU_AUTO_PDN_SEL	AL_SECOND					

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

05A0	RTC_AL_SEC	RTC Second Alarm Setting Register	0000

	SEL				AR											
Type	RW	RW		RO	WO	RW		RW	RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	K_EOSC32_VTCXO_ON_SEL	**The bit is only valid when EMBCK_SEL_MODE is set to EMB_K_EOSC32 mode.** 0: VTCXO controlled by HW 1: VTCXO always on
14:13	RTC_LPD_OPT	**f32k_ck_alive setting (rstb of LPSTA_RAW), depending on XOSC LPDETB (xosc32_ck_alive) or EOSC LPDETB (eosc32_ck_alive)** 2'b11: Always 1 2'b10: xosc32_ck_alive (trigger when clock stops) 2'b01: eosc32_ck_alive (trigger when VRTC low-V) 2'b00: xosc32_ck_alive & eosc32_ck_alive
12	BBPU_2SEC_STAT_STA	**Bbwakeup 1.6 sec status** 1'b0: 1.6 sec reboot did not happen before. 1'b1: 1.6 sec reboot happened before.
11	BBPU_2SEC_STAT_CLEAR	**Clears Bbwakeup 1.6 sec event** Read back as BBPU_2SEC_STAT.
10:9	BBPU_2SEC_MODE	2'b11: Never power down 2'b10: 1.6sec power down after battery is removed 2'b01: 0.6sec power down after battery is removed 2'b00: 0.1sec power down after battery is removed
8	BBPU_2SEC_EN	0: Legacy mode 1: 1.6sec power down mode
7	BBPU_2SEC_CK_SEL	0: embck_ck 1: eosc32_ck
6	BBPU_AUTO_PDN_SEL	0: Original 1.6sec reboot feature 1: Support both 1.6sec reboot and auto_pdn
5:0	AL_SECOND	**The second value of the alarm counter setting** Value range: 0~59

05A2	RTC_AL_MIN	RTC Minute Alarm Setting Register	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AL_MINUTE					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	AL_MINUTE	**The minute value of the alarm counter setting** Value range: 0~59

05A4	RTC_AL_HOU	RTC Hour Alarm Setting Register	0000

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

05A4 **RTC_AL_HOU** **RTC Hour Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE0											AL_HOUR				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE0	**NEW_SPARE0[7]:** WO: Reset bat status by writing 1, auto clear 0 NEW_SPARE0[6]: RO: 0 = no bat now; 1 = bat installed properly NEW_SPARE0[5]: RO: 0 = battery always exists; 1 = battery has been removed NEW_SPARE0[4:0]: Battery removed time counter; unit: minute; stopped when counting to 5'd30, reset to 0 by SPARE0[7]
4:0	AL_HOUR	**The hour value of the alarm counter setting** Value range: 0~23

05A6 **RTC_AL_DOM** **RTC Day-of-Month Alarm Setting Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE1											AL_DOM				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE1	**NEW_SPARE1[7:6]:** RO: spar_state[1:0] 2'b00: ST_PWR_OFF 2'b01: ST_PWR_ON 2'b10: ST_PWR_ON2OFF 2'b11: ST_SPAR_EN NEW_SPARE1[5]: RO: additional_spar_en 1'b0: No spar happend 1'b1: Spar happened NEW_SPARE1[4]: RO: uvlo_except_sync 1'b0: Battery voltage exceeds the UVLO threshold. 1'b1: Battery voltage is under the UVLO threshold. NEW_SPARE1[3]: RW: Alrarm clear method 1'b0: By SW 1'b1: By HW (xreset low -> high) NEW_SPARE1[2]: Reserved NEW_SPARE1[1]: RW: Autmatically SPAR/ALARM 1'b0: Clear by SW 1'b1: Clear SPAR/ALARM event in old legacy mode when SYSRST# transitions from high to low. NEW_SPARE1[0]: RW: Select triggering spar condition 1'b0: By UVLO

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1'b1: By 75kHz exist or not
4:0	AL_DOM	**The day-of-month value of the alarm counter setting** The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are 0.

05A8 RTC_AL_DOW RTC Day-of-Week Alarm Setting Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE2													AL_DOW		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE2	**Reserved for specific purposes**
2:0	AL_DOW	**The day-of-week value of the alarm counter setting** Value range: 1~7

05AA RTC_AL_MTH RTC Month Alarm Setting Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NEW_SPARE3												AL_MONTH			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15:8	NEW_SPARE3	**Reserved for specific purposes**
3:0	AL_MONTH	**The month value of the alarm counter setting** Value range: 1~12

05AC RTC_AL_YEA RTC Year Alarm Setting Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_K_EOSC_RSV									AL_YEAR						
Type	RW									RW						
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RTC_K_EOSC_RSV	**RTC_TEST_RSV[7]: VRTC_DDLO control** 0: DDLO_VRTC is gated by VTCXO0_EN. 1: DDLO_VRTC is not gated by VTCXO0_EN. RTC_TEST_RSV[6]: ENBB value in SW mode RTC_TEST_RSV[5]: ENBB mode selection 0: HW mode 1: SW mode (ENBB = RTC_TEST_RSV[6]) RTC_TEST_RSV[4]: VTCXO control in normal mode 0: Follow EOSC calibration control

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: Bypass EOSC calibration control RTC_TEST_RSV[3]: XOSC_EN and ENBB testmode selection 0: Normal mode 1: Testmode by GPI (XOSC_EN = GPI[3], ENBB = GPI[4]) RTC_TEST_RSV[2]: XOSC_EN value in SW mode RTC_TEST_RSV[1]: XOSC_EN mode selection 0: HW mode 1: SW mode (XOSC_EN = RTC_TEST_RSV[2]) RTC_TEST_RSV[0]: XOSC_EN configuration 0: XTAL less (XOSC_EN is always 1) 1: XTAL less within EOSC auto-calibration function
6:0	AL_YEAR	**The year value of the alarm counter setting** Value range: 0~127 (2000~2127)

05AE **RTC_OSC32_CON** **OSC32 Control** **0400**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_REG_XOSC32_ENB	RTC_GP_OSC32_CON		RTC_EOSC32_CHOP_EN	RTC_EOSC32_VCT_EN	RTC_GPS_CKOUT_EN	RTC_EMBCK_SEL_OPTION	RTC_EMBCK_SRC_SEL	RTC_EMBCK_SEL_MODE		RTC_XOSC32_ENB	XOSCCALI				
Type	RW	RW		RW	RW	RW	RW	RW	RW		RO	RW				
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RTC_REG_XOSC32_ENB	**XOSC32_ENB = 0 (32k crystal exists)** XOSC32_ENB = 1 (32k crystal does not exist.)
14:13	RTC_GP_OSC32_CON	**EOSC32 RSV registers** [14]: Select the clock source to GPS [13]: Adjust the current when eosc is powered up
12	RTC_EOSC32_CHOP_EN	**Enables EOSC32 chopper** When chopper is disabled, the current consumption can become lower. However, eosc32_ck might become unstable. When powerkeys do not matched, the chopper will be enabled. 0: Disable 1: Enable
11	RTC_EOSC32_VCT_EN	**Enables EOSC32 threshold tracking** 0: Disable 1: Enable
10	RTC_GPS_CKOUT_EN	**Powers up EOSC** When PAD_RTC_32K_2V8 is in the buffer mode, this bit is suggested to be set 1'b0 in order not to interfere the input clock. 1'b0: Power down 1'b1: Power up
9	RTC_EMBCK_SEL_OPTION	**Embedded clock selection option after battery removal** Note: Set this bit to 1'b1 to extend the embedded clock life time after battery removal with a poorer clock source. EOSC32 can only keep the spec before LPD. After LPD, the frequency drift will become larger. 0: Embedded clock switch back to dcxo decided by (eosc32_ck_alive & powerkey_match) 1: Embedded clock switch back to dcxo decided by (powerkey_match)

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
8	RTC_EMBCK_SRC_SEL	**Selects embedded clock source in EMB_K_EOSC32 mode (RTC_OSC32CON[7:6]=2'b01)** 0: f32k_ck src = dcxo_ck 1: f32k_ck src = eosc32_ck
7:6	RTC_EMBCK_SEL_MODE	**Embedded clock source selection mode** 00: EMB_SW_DCXO mode (from bit6). f32k_ck src = dcxo_ck 01: EMB_SW_EOSC32 mode(from bit6). f32k_ck src = eosc32_ck 10: EMB_K_EOSC32 mode. Initial f32k_ck source = DCXO; SW can configure f32k_ck src by configuring RTC_OSC32CON[8] (EMBCK_SEL). HW automatically switches f32k_ck src to eosc32_ck at VBAT LV level 11: EMB_HW (embedded HW) mode. Initial f32k_ck source = DCXO; HW automatically switches to EOSC32 at VBAT LV level.
5	RTC_XOSC32_ENB	**Read: XOSC32_ENB** Pin configuration of 32k crystal is used or not. 0: Use 32k crystal, f32k_ck source = XOSC32 1: No 32k crystal, f32k_ck source = embedded 32k sources (DCXO or EOSC32) Write: Manual clock during reloading, for debugging. SW can toggle this bit to generate SW clock. This clock is used as RTC registers' clock source only during reload procedure. When power-on without 32k's existence, this bit can be used to finish the reload procedure, then SW is capable of reading the RTC registers contents.
4:0	XOSCCALI	**GM calibration** Default: 4'b0111. The 2nd step is suggested to be 4'b0000. EOSC_CALI = charging cap calibration

05B0 **RTC_POWERKEY1** **RTC_POWERKEY1 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_POWERKEY1	

05B2 **RTC_POWERKEY2** **RTC_POWERKEY2 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_POWERKEY2	

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

05B4 RTC_PDN1 PDN1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PDN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_PDN1	Spare registers for software to keep power on and power off state information

05B6 RTC_PDN2 PDN2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PDN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_PDN2	Spare registers for software to keep power on and power off state information

05B8 RTC_SPAR0 Spare Register for Specific Purpose 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_SPAR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_SPAR0	Spare register for specific purpose 0

05BA RTC_SPAR1 Spare Register for Specific Purpose 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_SPAR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RTC_SPAR1	Spare register for specific purpose 1

05BC RTC_PROT Lock/Unlock Scheme to Prevent RTC Miswriting 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_PROT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description

15:0	RTC_PROT	**The RTC write interface is protected by RTC_PROT.**
		Whether the RTC writing interface is enabled or not is decided by RTC_PROT contents. When RTC_POWERKEY1 and RTC_POWERKEY2 are not equal to the correct values, the RTC writing interface will always be enabled. When they match, you have to perform the unlock flow to enable the writing interface.
		Unlock flow:
		1. *RTC_PROT=0x586a;
		2. *RTC_WRTGR=1;
		3. while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
		4. *RTC_PROT=0x9136;
		5. *RTC_WRTGR=1;
		6. while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
		Note: Always keep RTC in unlock state in power on mode. Once the normal RTC content writing is complete, do not modify the RTC_PROT content to lock RTC. The RTC_PROT contents will be cleared automatically when powered off immediately.

05BE **RTC_DIFF** **One-Time Calibration Offset** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALI_RD_SEL	K_EOSC32_RSV		POWER_DETECTED	RTC_DIFF											
Type	RW	RW		RO	RW											
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	CALI_RD_SEL	**Selects which RTC_CALI is to be read when RTC_CALI register is read** 0: Normal RTC_CALI 1: K_EOSC32_RTC_CALI
14	K_EOSC32_RSV	**Reserved bit for EMB_K_EOSC32 mode**
12	POWER_DETECTED	**Read new powerkey match status**
11:0	RTC_DIFF	**Adjusts internal counter of RTC** It affects once and returns to 0 when done. In some cases, observe the RTC is faster or slower than the standard. Changing RTC_TC_SEC is coarse and may cause alarm problem. RTC_DIFF provides a finer time unit. An internal 15-bit counter accumulates in each 32768Hz clock. Entering a non-zero value into RTC_DIFF causes the internal RTC counter to increase or decrease RTC_DIFF when RTC_DIFF changes to 0 again. RTC_DIFF represents as 2's complement form. For example, if you fill 0xfff into RTC_DIFF, the internal counter will decrease 1 when RTC_DIFF returns to 0. In other words, you can only use RTC_DIFF continuously if RTC_DIFF = 0 now. Note: RTC_DIFF ranges from 0x800 (-2048) to 0x7fd (2045). 0x7ff & 0x7fe are not allowed to use.

05C0 **RTC_CALI** **Repeat Calibration Offset** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

05C0	RTC_CALI	Repeat Calibration Offset	0000

Name	K_EOSC32_OVERFLOW	CALI_WR_SEL	RTC_CALI													
Type	RW	RW	RW													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	K_EOSC32_OVERFLOW	**EOSC32 calibration overflow (EOSC32 RTC_CALI update result from PMU rtc_eosc_cali module overflow)** 0: Not overflow 1: Overflow
14	CALI_WR_SEL	**Enables EOSC32 cali value write** Only takes effect in RTC_CALI write operation. 0: Normal RTC_CALI 1: K_EOSC32_RTC_CALI
13:0	RTC_CALI	**These registers provide a repeat calibration scheme.** RTC_CALI provides two types of calibration: 1. 7-bit calibration capability in 8-second duration, i.e. 5-bit calibration capability in each second. RTC_CALI represents in 2's complement form, such that you can adjust RTC to be increasing or decreasing. Due to RTC_CALI is revealed in 8 seconds, the resolution is less than a 1/32768 clock. Avg. resolution: 1/32768/8 = 3.81us Avg. adjust range: -0.244~0.240ms/sec in 2's complement: -0x40~0x3f (-64~63) 2. 14-bit calibration capability in 1-second duration at EMB_K_EOSC32 mode (K_EOSC32_RTC_CALI); this usage is with resolution 1/32768=30.52us.

05C2	RTC_WRTGR	Enable Transfers from Core to RTC in Queue	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WRTGR
Type																WO
Reset																0

Bit(s)	Name	Description
0	WRTGR	**This register enables the transfers from core to RTC.** After you modify all the RTC registers you are to change, write RTC_WRTGR to 1 to trigger the transfer. The prior writing operations are queued at core power domain. The pending data will not be transferred to RTC domain until WRTGR=1. After WRTGR=1, the pending data are transferred to RTC domain sequentially in order of register address, from low to high. For example: RTC_BBPU -> RTC_IRQ_EN -> RTC_CII_EN -> RTC_AL_MASK -> RTC_TC_SEC -> etc. The CBUSY in RTC_BBPU is equal to 1 in writing process. You can observe CBUSY to determine when the transmission is completed.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

05C4 RTC_CON Other RTC Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPSTA_RAW	GPI	GE8	GE4	GPU	GPEN	GSMT	GSR	GOE	GPO	F32KOB	CDBO	LPRST	XOSC32_LPEN	EOSC32_LPEN	VBAT_LPSTA_RAW
Type	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	LPSTA_RAW	**Raw status of LP_STA** You can re-initialize LPD to clear this bit. Note: This bit is always high before LPD initialization sequence after the first power-on.
14	GPI	**Input value of RTC_GPIO when GOE=0 (input mode)**
13	GE8	**Driving capability of RTC_GPIO**
12	GE4	**Driving capability of RTC_GPIO**
11	GPU	**Pull-up of RTC_GPIO**
10	GPEN	**Pull enable of RTC_GPIO** When GPEN=1, RTC_GPIO will pull up if GPU=1; pull down if GPU=0.
9	GSMT	**SMT of RTC_GPIO** Control pin for Schmitt trigger circuit. 0: RTC_GPIO Schmitt trigger off 1: RTC_GPIO Schmitt trigger on
8	GSR	**SR of RTC_GPIO** Output slew rate control. High asserted. SR=0, slower slew. SR=1. 0: RTC_GPIO higher slew output 1: RTC_GPIO slower slew output
7	GOE	**OE of RTC_GPIO** 1'b0: RTC_GPIO is in input mode 1'b1: RTC_GPIO is in output mode
6	GPO	**Output value of RTC_GPIO when OE=1 and COREDETB=0.** Selects to output pdn_flat_out signal or tick_sec to RTC_GPIO when OE=1 and COREDETB=1.
5	F32KOB	**Exports 32.768kHz clock on RTC_GPIO in analog IO mode** 1'b0: Analog IO mode 1'b1: Digital IO mode
4	CDBO	**Exports signal on RTC_GPIO** 1'b0: Exports GPO value 1'b1: When LPD_OPT=1, export LPDETB. When LPD_OPT=0 and GPO=0, export pdn_flat_out signal. When LPD_OPT=0 and GPO=1, export tick_sec.
3	LPRST	**Resets LPDETB** This only takes effect when LPEN=1. When LPEN=0, the internal LPRST signal to XOSC32 is always 0.
2	XOSC32_LPEN	**Enables XOSC LPDETB function** LP initialization sequence: 1. Write XOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. wait cbusy down. 2. Write XOSC32_LPEN = 1, LPRST = 1. Write RTC_WRTGR = 1. wait cbusy down. 3. Write XOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. wait cbusy down. The XOSC32 LPD occurs when 32k stops. It can be applied at both XOSC32 and EOSC32.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
1	EOSC32_LPEN	**Enables EOSC LPDETB function** LP initialization sequence: 1. Write EOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. wait cbusy down. 2. Write EOSC32_LPEN = 1, LPRST = 1. Write RTC_WRTGR = 1. wait cbusy down. 3. Write EOSC32_LPEN = 1, LPRST = 0. Write RTC_WRTGR = 1. wait cbusy down. The EOSC32 LPD occurs at VRTC~=1.25V. It can be applied at both XOSC32 and EOSC32.
0	VBAT_LPSTA_RAW	**Indicates the battery has been in LP state** When the embedded hardware mode is used, the flag also indicates that hardware has switched clock source from DCXO to EOSC32. Software needs to clear this bit for the next use. Note: VBAT LP state = VBAT < 2.5V (DDLO) 0: VBAT has not been in LP state. 1: VBAT has been in LP state.

0608 **RTC_TC_SEC_SEC** **Security RTC Seconds Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_SECOND_SEC					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_SECOND_SEC	**The second initial value for the time counter** Value range: 0~59

060A **RTC_TC_MIN_SEC** **Security RTC Minutes Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TC_MINUTE_SEC					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	TC_MINUTE_SEC	**The minute initial value for the time counter** Value range: 0~59

060C **RTC_TC_HOU_SEC** **Security RTC Hours Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_HOUR_SEC				
Type												RW				
Reset												0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
4:0	TC_HOUR_SEC	**Hour initial value for the time counter** Value range: 0~23

060E **RTC_TC_DOM_SEC** **Security RTC Day-of-Month Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TC_DOM_SEC				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TC_DOM_SEC	**The day-of-month initial value for the time counter** The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are 0.

0610 **RTC_TC_DOW_SEC** **Security RTC Day-of-Week Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														TC_DOW_SEC		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	TC_DOW_SEC	**The day-of-week initial value for the time counter** Value range: 1~7

0612 **RTC_TC_MTH_SEC** **Security RTC Month Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TC_MONTH_SEC			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TC_MONTH_SEC	**The month initial value for the time counter** Value range: 1~12

0614 **RTC_TC_YEA_SEC** **Security RTC Year Time Counter Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TC_YEAR_SEC						
Type										RW						
Reset										0	0	0	0	0	0	0

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
6:0	TC_YEAR_SEC	**The year initial value for the time counter** Value range: 0~127 (2000~2127). Software can bias the year as multiples of 4 for the internal leap-year formula, e.g. 2000~2127, 1972~2099, 1904~2031. To simplify, RTC hardware treats all 4-multiple as leap years. If the range you define includes non-leap 4-multiple year (e.g. 2100), adjust to correct date by yourself (e.g. change Feb. 29th, 2100 to Mar. 1st, 2100). It is suggested to bias the range large than 1900 and less than 2100 to evade the manual adjusting, i.e. the bias values are suggested to be in the range of [-28,-96], that are (1972~2099) ~ (1904~2031). Formal leap formula: if year modulo 400 is 0 then leap else if year modulo 100 is 0 then no_leap else if year modulo 4 is 0 then leap else no_leap

0616 **RTC_SEC_CK_PDN** **Security RTC Clock Control Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RTC_SEC_CK_PDN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RTC_SEC_CK_PDN	**Security RTC clock control** 0: Turn off clock 1: Turn on clock

0618 **RTC_SEC_WRTGR** **Enable Transfers from Core to Security RTC in Queue** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RTC_SEC_WRTGR
Type																WO
Reset																0

Bit(s)	Name	Description
0	RTC_SEC_WRTGR	**This register enables the transfers from core to security RTC.** After you modify all the RTC registers you are to change, write RTC_WRTGR to 1 to trigger the transfer. The prior writing operations are queued at core power domain. The pending data will not be transferred to RTC domain until WRTGR=1. After WRTGR=1, the pending data will be transferred to RTC domain sequentially in order of register address, from low to high. For example:

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		RTC_TC_SEC_SEC -> RTC_TC_MIN_SEC -> RTC_TC_HOU_SEC etc.

0788 **DCXO_CW00** **DCXO Code Word 0** **6B6D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CLKSEL_MAN	XO_ENBB_EN_M	XO_ENBB_MAN	XO_BB_LPM_EN	XO_EXTBUF4_EN_M	XO_EXTBUF4_MODE		XO_EXTBUF3_EN_M	XO_EXTBUF3_MODE		XO_EXTBUF2_EN_M	XO_EXTBUF2_MODE		XO_EXTBUF1_EN_M	XO_EXTBUF1_MODE	
Type	RW	RW	RW	RW	RW	RW		RW	RW		RW	RW		RW	RW	
Reset	0	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1

Bit(s)	Name	Description
15	XO_CLKSEL_MAN	0: XO2~4 are controlled by pin (CLK_SEL). 1: XO2~4 are controlled by register XO_CLKSEL_MAN_EN (default)
14	XO_ENBB_EN_M	0: XO_SOC will be disabled if manual (register) control 1: XO_SOC will be enabled if manual (register) control (default)
13	XO_ENBB_MAN	0: XO_SOC is controlled by pin (EN_BB). 1: XO_SOC is controlled by register XO_ENBB_MAN_EN (default)
12	XO_BB_LPM_EN	**SW controlled LPM for saving power during transceiver standby** Must be EN_BB=1, CLK_SEL=0.
11	XO_EXTBUF4_EN_M	**Enables/Disables XO_CEL during manual (register) control**
10:9	XO_EXTBUF4_MODE	00: Register controlled by XO_EXTBUF4_EN_M 01: EN_BB 10: CLK_SEL 11: XO_EXTBUF2_EN_M or XO_EXTBUF3_EN_M or CLK_SEL
8	XO_EXTBUF3_EN_M	**Enables/Disables XO_NFC during manual (register) control**
7:6	XO_EXTBUF3_MODE	00: Register controlled by XO_EXTBUF3_EN_M 01: EN_BB 10: CLK_SEL 11: XO_EXTBUF2_EN_M or XO_EXTBUF3_EN_M or CLK_SEL
5	XO_EXTBUF2_EN_M	**Enables/Disables XO_WCN during manual (register) control**
4:3	XO_EXTBUF2_MODE	00: Register controlled by XO_EXTBUF2_EN_M 01: EN_BB 10: CLK_SEL 11: XO_EXTBUF2_EN_M or XO_EXTBUF3_EN_M or CLK_SEL
2	XO_EXTBUF1_EN_M	**Enables/Disables XO_SOC during manual (register) control**
1:0	XO_EXTBUF1_MODE	00: Register controlled by XO_EXTBUF1_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL

078A **DCXO_CW00_SET** **DCXO Code Word 0 Set** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

078A DCXO_CW00_SET DCXO Code Word 0 Set 0000

Name	DCXO_CW00_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW00_SET	**Sets up DCXO Code Word 0** 0: No set 1: Set

078C DCXO_CW00_CLR DCXO Code Word 0 Clear 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW00_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW00_CLR	**DCXO Code Word 0 Clear** 0: No clear 1: Clear

078E DCXO_CW01 DCXO Code Word 1 6D55

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BBLPM_CKSEL_M	XO_LPBUF_EN_M	XO_LPM_PREBUF_EN_M	XO_LPMBUF_MAN	XO_IBUF_EN_M	XO_PBUF_EN_M	XO_INTBUF_MAN	XO_EXTBUF4_CKG_EN_M	XO_EXTBUF4_CKG_MAN	XO_EXTBUF3_CKG_EN_M	XO_EXTBUF3_CKG_MAN	XO_EXTBUF2_CKG_EN_M	XO_EXTBUF2_CKG_MAN	XO_EXTBUF1_CKG_EN_M	XO_EXTBUF1_CKG_MAN	XO_CLKSEL_EN_M
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	XO_BBLPM_CKSEL_M	**XO_WCN and XO_CEL LPM frequency manually switched if XO_LPMBUF_MAN=1**
14	XO_LPBUF_EN_M	**XO low power buffer manually enable if XO_LPMBUF_MAN=1**
13	XO_LPM_PREBUF_EN_M	**XO low power buffer bias manually enable if XO_LPMBUF_MAN=1**
12	XO_LPMBUF_MAN	**XO low power buffer enable manual mode**
11	XO_IBUF_EN_M	**XO isolated buffer manually enable if XO_INTBUF_MAN=1**
10	XO_PBUF_EN_M	**XO pre-buffer manually enable if XO_INTBUF_MAN=1**
9	XO_INTBUF_MAN	**XO internal buffer enable manual mode**
8	XO_EXTBUF4_CKG_EN_M	**XO_CEL 26MHz output enable while manual mode**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
7	XO_EXTBUF4_CKG_MAN	**XO_CEL 26MHz output enable manual mode**
6	XO_EXTBUF3_CKG_EN_M	**XO_NFC 26MHz output enable while manual mode**
5	XO_EXTBUF3_CKG_MAN	**XO_NFC 26MHz output enable manual mode**
4	XO_EXTBUF2_CKG_EN_M	**XO_WCN 26MHz output enable while manual mode**
3	XO_EXTBUF2_CKG_MAN	**XO_WCN 26MHz output enable manual mode**
2	XO_EXTBUF1_CKG_EN_M	**XO_SOC 26MHz output enable while manual mode**
1	XO_EXTBUF1_CKG_MAN	**XO_SOC 26MHz output enable manual mode**
0	XO_CLKSEL_EN_M	0: XO2~4 will be disabled if manual (register) control 1: XO2~4 will be enabled if manual(register) control (default)

0790 **DCXO_CW02** **DCXO Code Word 2** **386A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BUFLDOK_EN	XO_26MLP_MAN_EN	XO_CBANK_SYNC_DYN	XO_LDOCAL_EN	XO_EN26M_OFFSQ_EN	XO_AAC_MODE_FPM		XO_AAC_MODE_LPM		XO_AAC_FPM_TIME		XO_STRUP_MODE	XO_XMODE_M	XO_XMODE_MAN	XO_EN32K_M	XO_EN32K_MAN
Type	RW	RW	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW
Reset	0	0	1	1	1	0	0	0	0	1	1	0	1	0	1	0

Bit(s)	Name	Description
15	XO_BUFLDOK_EN	**SW trigger external buffer LDO calibration**
14	XO_26MLP_MAN_EN	**Set high to always enable XO low power 26M to digital**
13	XO_CBANK_SYNC_DYN	0: Update clock of CBANK always turned on 1: Update clock of CBANK only turned on during CDAC update (default)
12	XO_LDOCAL_EN	0: Keep previous FPMLDO voltage setting 1: Trigger FPMLDO calibration (binary search) when entering FPM (default)
11	XO_EN26M_OFFSQ_EN	**Enables OFF sequence when 26M_EN=0**
10:9	XO_AAC_MODE_FPM	00: AAC 1st + 2nd steps (default) 01: Bypass and reuse previous value 10: AAC 1st only 11: Manual control bypass AAC
8:7	XO_AAC_MODE_LPM	00: AAC 1st + 2nd steps (default) 01: Bypass and reuse previous value 10: AAC 1st only 11: Manual control bypass AAC
6:5	XO_AAC_FPM_TIME	00: 16T32K 01: 32T32K 10: 64T32K 11: 128T32K (default)
4	XO_STRUP_MODE	0: Open OR close detection (default)

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: Open AND close detection
3	XO_XMODE_M	0: XMODE_G will be disabled if manual (register) control 1: XMODE_G will be enabled if manual (register) control (default)
2	XO_XMODE_MAN	0: XMODE_G is controlled by pin (XMODE). (default) 1: XMODE_G is controlled by register XO_XMODE_M.
1	XO_EN32K_M	0: EN_32K_G will be disabled if manual (register) control 1: EN_32K_G will be enabled if manual (register) control (default)
0	XO_EN32K_MAN	0: EN_32K_G is controlled by pin (XO32K_EN). (default) 1: EN_32K_G is controlled by register XO_EN32K_M.

0792 **DCXO_CW03** **DCXO Code Word 3** **842B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_FPM_ISEL_MAN					XO_LPM_ISEL_MAN					XO_EXTBUF7_CKG_EN_M	XO_EXTBUF7_CKG_MAN	XO_EXTBUF6_CKG_EN_M	XO_EXTBUF6_CKG_MAN	XO_PMU_CKEN_MAN	XO_PMU_CKEN_M
Type	RW					RW					RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1

Bit(s)	Name	Description
15:11	XO_FPM_ISEL_MAN	XO core FPM current settings if XO_AAC_MODE_LPM=11
10:6	XO_LPM_ISEL_MAN	XO core LPM current settings if XO_AAC_MODE_FPM=11
5	XO_EXTBUF7_CKG_EN_M	XO_EXT 26MHz output enable while manual mode
4	XO_EXTBUF7_CKG_MAN	XO_EXT 26MHz output enable manual mode
3	XO_EXTBUF6_CKG_EN_M	XO_PD 26MHz output enable while manual mode
2	XO_EXTBUF6_CKG_MAN	XO_PD 26MHz output enable manual mode
1	XO_PMU_CKEN_MAN	PMU 26M clock enable manual mode
0	XO_PMU_CKEN_M	PMU 26M clock manual control

0794 **DCXO_CW04** **DCXO Code Word 4** **FF55**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CDAC_LPM								XO_CDAC_FPM							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:8	XO_CDAC_LPM	XO CDAC code (complement) during LPM
7:0	XO_CDAC_FPM	XO CDAC code (complement) during FPM

0796 DCXO_CW05 DCXO Code Word 5 DD40

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_FPM		XO_32KDIV_NFRAC_FPM													
Type	RW		RW													
Reset	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	XO_COFST_FPM	XO CDAC offset code during FPM
13:0	XO_32KDIV_NFRAC_FPM	32K divider fractional input during FPM

0798 DCXO_CW06 DCXO Code Word 6 2318

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_LPM		XO_32KDIV_NFRAC_LPM													
Type	RW		RW													
Reset	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
15:14	XO_COFST_LPM	XO CDAC offset code during LPM
13:0	XO_32KDIV_NFRAC_LPM	32K divider fractional input during LPM

079A DCXO_CW07 DCXO Code Word 7 8FFE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CORE_IDAC_FPM		XO_CORE_GMX2_FPM	XO_CORE_BYPCAS_FPM	XO_ILPM_COMP_EN_M	XO_IFPM_COMP_EN_M	XO_IAAC_COMP_EN_M	XO_VTCGEN_EN_M	XO_LPMBIAS_EN_M	XO_CORE_VBLPM_EN_M	XO_CORE_VBFPM_EN_M	XO_STARTUP_EN_M	XO_CORE_AAC_EN_M	XO_CORE_TURBO_EN_M	XO_CORE_EN_M	XO_CORE_MAN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Name	Description
15:14	XO_CORE_IDAC_FPM	XO gm core current control during FPM or XO_CORE_MAN=1
13	XO_CORE_GMX2_FPM	XO core Gm double option during FPM or XO_CORE_MAN=1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
12	XO_CORE_BYPCAS_FPM	XO core bypass cascode option during FPM or XO_CORE_MAN=1
11	XO_ILPM_COMP_EN_M	XO ILPM to comparator enable if XO_CORE_MAN=1
10	XO_IFPM_COMP_EN_M	XO IFPM to comparator enable if XO_CORE_MAN=1
9	XO_IAAC_COMP_EN_M	XO IAAC to comparator enable if XO_CORE_MAN=1
8	XO_VTCGEN_EN_M	FPM gm bias circuit enable if XO_CORE_MAN=1
7	XO_LPMBIAS_EN_M	XO core LPM bias circuit enable if XO_CORE_MAN=1
6	XO_CORE_VBLPM_EN_M	XO core LPM bias enable if XO_CORE_MAN=1
5	XO_CORE_VBFPM_EN_M	XO core FPM bias enable if XO_CORE_MAN=1
4	XO_STARTUP_EN_M	XO core startup gating option if XO_CORE_MAN=1
3	XO_CORE_AAC_EN_M	XO core AAC bias enable if XO_CORE_MAN=1
2	XO_CORE_TURBO_EN_M	XO core iturbo option if XO_CORE_MAN=1
1	XO_CORE_EN_M	XO oscillator core enable if XO_CORE_MAN=1
0	XO_CORE_MAN	XO core manual mode

079C **DCXO_CW08** **DCXO Code Word 8** **46BE**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AAC_COMP_POL	XO_AAC_VSEL_FPM				XO_AAC_COMP_HV_FPM	XO_AAC_VOFST_FPM		XO_AAC_IBIAS_FPM		XO_AAC_HV_FPM	XO_COMP_TSTEN_M	XO_COMP_EN_M	XO_AAC_MONEN_M	XO_AAC_EN_M	XO_AAC_COMP_MAN
Type	RW	RW				RW	RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	0

Bit(s)	Name	Description
15	XO_AAC_COMP_POL	Inverts polarity of AD_XO_AAC_COMP_OUT for mistake in case
14:11	XO_AAC_VSEL_FPM	XO AAC target peak-to-peak amplitude during FPM or XO_AAC_COMP_MAN=1
10	XO_AAC_COMP_HV_FPM	XO AAC COMP high amplitude mode during FPM or XO_AAC_COMP_MAN=1
9:8	XO_AAC_VOFST_FPM	XO AAC input offset settings during FPM or XO_AAC_COMP_MAN=1
7:6	XO_AAC_IBIAS_FPM	XO AAC bias current settings during FPM or XO_AAC_COMP_MAN=1
5	XO_AAC_HV_FPM	XO AAC high amplitude mode during FPM or XO_AAC_COMP_MAN=1
4	XO_COMP_TSTEN	XO COMP voltage testing mode during startup or XO_AAC_COMP_MAN=1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	_M	
3	XO_COMP_EN_M	XO COMP enable during AAC or XO_AAC_COMP_MAN=1
2	XO_AAC_MONEN_M	XO AAC voltage monitor mode during startup or XO_AAC_COMP_MAN=1
1	XO_AAC_EN_M	XO AAC enable during AAC or XO_AAC_COMP_MAN=1
0	XO_AAC_COMP_MAN	XO AAC/COMP manual mode

079E **DCXO_CW09** **DCXO Code Word 9** **010F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_SWRST	XO_AAC_FPM_SWEN	XO_AAC_VOFST_LPM		XO_AAC_IBIAS_LPM		XO_AAC_HV_LPM	XO_AAC_VSEL_LPM				XO_AAC_COMP_HV_LPM	XO_CORE_IDAC_LPM		XO_CORE_GMX2_LPM	XO_CORE_BYPCAS_LPM
Type	RW	RW	RW		RW		RW	RW				RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
15	XO_SWRST	**XO digital macro software reset**
14	XO_AAC_FPM_SWEN	0: Disable 1: SW trigger AAC during FPM
13:12	XO_AAC_VOFST_LPM	**XO AAC input offset settings during LPM**
11:10	XO_AAC_IBIAS_LPM	**XO AAC bias current settings during LPM**
9	XO_AAC_HV_LPM	**XO AAC high amplitude mode during LPM**
8:5	XO_AAC_VSEL_LPM	**XO AAC target peak-to-peak amplitude during LPM**
4	XO_AAC_COMP_HV_LPM	**XO AAC COMP high amplitude mode during LPM**
3:2	XO_CORE_IDAC_LPM	**XO gm core current control during LPM**
1	XO_CORE_GMX2_LPM	**XO core Gm double option during LPM**
0	XO_CORE_BYPCAS_LPM	**XO core bypass cascode option during LPM**

07A0 **DCXO_CW10** **DCXO Code Word 10** **EF50**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_VBIST_EN_M	XO_TEST_VCAL_EN_M	XO_LDOVTST_EN_M	XO_LDOPBUF_VSET_M				XO_LDOPBUF_EN_M	XO_LDO_MAN	XO_CTL_SYNC_EN_M	XO_CTL_SYNC_MAN	XO_CBANK_SYNC_EN_M	XO_CBANK_SYNC_MAN	XO_32K_DIV_TEST_EN	XO_32K_DIV_RATIO_MAN	XO_32K_DIV_SWRST

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Type	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
15	XO_VBIST_EN_M	XO self voltage calibration monitor path enable if XO_LDO_MAN=1
14	XO_TEST_VCAL_EN_M	XO self voltage calibrated mode enable if XO_LDO_MAN=1
13	XO_LDOVTST_EN_M	XO PBUF LDO voltage testmux enable if XO_LDO_MAN=1
12:9	XO_LDOPBUF_VSET_M	XO PBUF LDO output voltage manual settings if XO_LDO_MAN=1
8	XO_LDOPBUF_EN_M	XO internal buffer bias enable if XO_LDO_MAN=1
7	XO_LDO_MAN	XO LDO enable manual mode
6	XO_CTL_SYNC_EN_M	CTL SYNC enable if XO_SYNC_MAN=1
5	XO_CTL_SYNC_MAN	XO local CTL sync enable manual mode
4	XO_CBANK_SYNC_EN_M	CBANK SYNC enable if XO_CBANK_SYNC_MAN=1
3	XO_CBANK_SYNC_MAN	XO local CBANK sync enable manual mode
2	XO_32KDIV_TEST_EN	DCXO 32K divider testing output thru DCXO_AUXOUT
1	XO_32KDIV_RATIO_MAN	Manually control set the ratio of 32K divider high
0	XO_32KDIV_SWRST	32k digital divider software reset

07A2 **DCXO_CW11** **DCXO Code Word 11** **AD00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**XO_BUF1LDO_CAL_M**	**XO_BUFLDOK_MAN**	**XO_EXTBUF7_EN_M**	**XO_EXTBUF7_MODE**		**XO_EXTBUF6_EN_M**	**XO_EXTBUF6_MODE**		**XO_RESERVED3**			**XO_VTEST_SEL_MUX**				
Type	RW	RW	RW	RW		RW	RW		RW			RW				
Reset	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	XO_BUF1LDO_CAL_M	**Enables/Disables BUF1LDO CAL during manual (register) control**
14	XO_BUFLDOK_MAN	**EXTBUF LDO CAL enable manual mode**
13	XO_EXTBUF7_EN_M	**Enables/Disables XO_EXT during manual (register) control**
12:11	XO_EXTBUF7_MODE	00: Register controlled by XO_EXTBUF7_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL
10	XO_EXTBUF6_EN	**Enables/Disables XO_PD during manual (register) control**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	_M	
9:8	XO_EXTBUF6_MODE	00: Register controlled by XO_EXTBUF6_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL
7:5	XO_RESERVED3	**Register reserved**
4:0	XO_VTEST_SEL_MUX	**XO testmux selection MUX**

07A4 DCXO_CW11_SET DCXO Code Word 11 Set 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW11_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW11_SET	**Sets up DCXO Code Word 11** 0: No set 1: Set

07A6 DCXO_CW11_CLR DCXO Code Word 11 Clear 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW11_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW11_CLR	**Clears DCXO Code Word 11** 0: No clear 1: Clear

07A8 DCXO_CW12 DCXO Code Word 12 8A75

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_LDOPBUF_ENCL	RG_XO_LDOPBUF_BYP	RG_XO_LPBUF_INV	RG_XO_CTL_SYNC_BYP	RG_XO_CTL_POL	RG_XO_CBANK_SYNC_BYP	RG_XO_CBANK_POL	RG_XO_SYNC_CKPOL	XO_THADC_EN	RG_XO_CORE_OSCTD		XO_CAL_EN_M	XO_CAL_EN_MAN	XO_VIO18PG_BUFEN	XO_EXTBUF4_CLKSEL_MAN	XO_BUFLDO_CAL_M
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW
Reset	1	0	0	0	1	0	1	0	0	1	1	1	0	1	0	1

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15	RG_XO_LDOPBUF_ENCL	**Enable signal for XO PBUFLDO closed loop**
14	RG_XO_LDOPBUF_BYP	**Enable signal for XO PBUFLDO bypass mode**
13	RG_XO_LPBUF_INV	**XO control signal of clock inversion for low power buffer chain**
12	RG_XO_CTL_SYNC_BYP	**XO control signal for bypassing bias control local synchronization**
11	RG_XO_CTL_POL	**XO control signal of clock polarity for bias control local synchronization** 0: Positive edge 1: Falling edge
10	RG_XO_CBANK_SYNC_BYP	**XO control signal for bypassing CBank control local synchronization**
9	RG_XO_CBANK_POL	**XO control signal of clock polarity for CBank control local synchronization** 0: Positive edge 1: Falling edge
8	RG_XO_SYNC_CKPOL	**XO control signal of local synchronized clock polarity** 0: In-phase of X1 1: Out-of-phase of X1
7	XO_THADC_EN	**Enables Vbe monitor by AUXADC** For XO temperature sensing.
6:5	RG_XO_CORE_OSCTD	**DCXO control signal for startup delay controls (open-loop)**
4	XO_CAL_EN_M	**CAL_EN manual enable when XO_CAL_EN_MAN=1**
3	XO_CAL_EN_MAN	**CAL_EN manual control mux**
2	XO_VIO18PG_BUFEN	**Buffer enable is gated by VIO18_PG or not**
1	XO_EXTBUF4_CLKSEL_MAN	0: Enable/Disable XO_CEL from pin control 1: Enable/Disable XO_CEL from register
0	XO_BUFLDO_CAL_M	**Enables/Disables BUFLDO CAL during manual (register) control**

07AA **DCXO_CW13** **DCXO Code Word 13** **9829**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_XO_BUFLDO24_IBX2	RG_XO_BUFLDO24_ENCL	RG_XO_VOW_DIV		RG_XO_VOW_EN			RG_XO_IBUF_ISET		RG_XO_PBUF_ISET		RG_XO_VGBIAS_VSET	
Type				RW	RW	RW		RW			RW		RW		RW	
Reset				1	1	0	0	0			1	0	1	0	0	1

Bit(s)	Name	Description
12	RG_XO_BUFLDO24_IBX2	**XO control signal of bias current doubler on EXTBUF24 LDO**
11	RG_XO_BUFLDO24_ENCL	**Enable signal of EXTBUF24 LDO closed loop**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
10:9	RG_XO_VOW_DIV	00: 26M 01: 26M/2 10: 26M/4 11: 26M/8
8	RG_XO_VOW_EN	**26MHz clk for VOW use**
5:4	RG_XO_IBUF_ISET	**XO control signal of internal isolated buffer current**
3:2	RG_XO_PBUF_ISET	**XO control signal of FPM pre-buffer current**
1:0	RG_XO_VGBIAS_VSET	**XO input gate bias control during FPM**

07AC **DCXO_CW14** **DCXO Code Word 14** **A2B5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_AUDIO_ATTEN		XO_AUDIO_EN_M	XO_EXTBUF2_CLKSEL_MAN		RG_XO_EXTBUF_INV	RG_XO_LVLDO_RFB		RG_XO_BUFLDO67_IX2	RG_XO_BUFLDO67_IBX2	RG_XO_BUFLDO67_ENCL	RG_XO_LVLDO_I_CTRL		RG_XO_BUFLDO13_IX2	RG_XO_BUFLDO13_IBX2	RG_XO_BUFLDO13_ENCL
Type	RW		RW	RW		RW	RW		RW	RW	RW	RW		RW	RW	RW
Reset	1	0	1	0		0	1	0	1	0	1	1	0	1	0	1

Bit(s)	Name	Description
15:14	RG_XO_AUDIO_ATTEN	XO control signal of RC filter on LP path
13	XO_AUDIO_EN_M	XO_AUDIO_EN_M
12	XO_EXTBUF2_CLKSEL_MAN	XO_EXTBUF2_CLKSEL_MAN
10	RG_XO_EXTBUF_INV	XO control signal of clock inversion for low noise external buffer
9:8	RG_XO_LVLDO_RFB	Selects LVLDO Vout
7	RG_XO_BUFLDO67_IX2	XO control signal of double current on EXTBUF67 LDO
6	RG_XO_BUFLDO67_IBX2	XO control signal of bias current doubler on EXTBUF67 LDO
5	RG_XO_BUFLDO67_ENCL	Enable signal of EXTBUF67 LDO closed loop
4:3	RG_XO_LVLDO_I_CTRL	LVLDO current sel
2	RG_XO_BUFLDO13_IX2	XO control signal of double current on EXTBUF13 LDO
1	RG_XO_BUFLDO13_IBX2	XO control signal of bias current doubler on EXTBUF13 LDO
0	RG_XO_BUFLDO13_ENCL	Enable signal of EXTBUF13 LDO closed loop

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

07AE DCXO_CW15 DCXO Code Word 15 A19A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_EXTBUF7_HD		RG_XO_EXTBUF6_HD				RG_XO_EXTBUF4_HD		RG_XO_EXTBUF3_HD		RG_XO_EXTBUF2_HD		RG_XO_EXTBUF1_HD		RG_XO_AUDIO_ISET	
Type	RW		RW				RW		RW		RW		RW		RW	
Reset	1	0	1	0			0	1	1	0	0	1	1	0	1	0

Bit(s)	Name	Description
15:14	RG_XO_EXTBUF7_HD	XO control signal of EXTBUF7 output driving strength
13:12	RG_XO_EXTBUF6_HD	XO control signal of EXTBUF6 output driving strength
9:8	RG_XO_EXTBUF4_HD	XO control signal of EXTBUF4 output driving strength
7:6	RG_XO_EXTBUF3_HD	XO control signal of EXTBUF3 output driving strength
5:4	RG_XO_EXTBUF2_HD	XO control signal of EXTBUF2 output driving strength
3:2	RG_XO_EXTBUF1_HD	XO control signal of EXTBUF1 output driving strength
1:0	RG_XO_AUDIO_ISET	XO control signal of LP buffer current

07B0 DCXO_CW16 DCXO Code Word 16 A8AA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_LPM_PREBUF_ISET		XO_EXTBUF7_ISET_M		XO_EXTBUF6_ISET_M				XO_EXTBUF4_ISET_M		XO_EXTBUF3_ISET_M		XO_EXTBUF2_ISET_M		XO_EXTBUF1_ISET_M	
Type	RW		RW		RW				RW		RW		RW		RW	
Reset	1	0	1	0	1	0			1	0	1	0	1	0	1	0

Bit(s)	Name	Description
15:14	RG_XO_LPM_PREBUF_ISET	Current settings for 26MHz low power pre-buffer
13:12	XO_EXTBUF7_ISET_M	XO control signal of current on EXTBUF7
11:10	XO_EXTBUF6_ISET_M	XO control signal of current on EXTBUF6
7:6	XO_EXTBUF4_ISET_M	XO control signal of current on EXTBUF4
5:4	XO_EXTBUF3_ISET_M	XO control signal of current on EXTBUF3
3:2	XO_EXTBUF2_ISET_M	XO control signal of current on EXTBUF2
1:0	XO_EXTBUF1_ISET_M	XO control signal of current on EXTBUF1

07B2 DCXO_CW17 DCXO Code Word 17 7773

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BUFLDO67_VSET_M				XO_BUFLDO24_VSET_M				XO_BUFLDO13_VSET_M				RG_XO_TSOURCE_EN	XO_THADC_EN_MAN		
Type	RW				RW				RW				RW	RW		
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	0		

Bit(s)	Name	Description
15:12	XO_BUFLDO67_VSET_M	XO control signal of EXTBUF67 LDO voltage
11:8	XO_BUFLDO24_VSET_M	XO control signal of EXTBUF24 LDO voltage
7:4	XO_BUFLDO13_VSET_M	XO control signal of EXTBUF13 LDO voltage
3	RG_XO_TSOURCE_EN	Enables thermal source for thermal calibration
2	XO_THADC_EN_MAN	THADC enable manual mode

07B8 DCXO_CW20 DCXO Code Word 20 0011

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_XO_HEATER_SEL		
Type														RW		
Reset														0	0	

Bit(s)	Name	Description
2:1	RG_XO_HEATER_SEL	

07BA DCXO_CW21 DCXO Code Word 21 02A7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_XO_CORNER_SETTING_TUNE									
Type							RW									
Reset							1	0	1	0	1	0	0	1	1	1

Bit(s)	Name	Description
9:0	RG_XO_CORNER_SETTING_TUNE	

07BC DCXO_CW22 DCXO Code Word 22 0280

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Name							XO_PTATCTAT_EN_FPM	XO_PTATCTAT_EN_LPM	XO_PTATCTAT_EN_M	XO_PTATCTAT_EN_MAN						
Type							RW	RW	RW	RW						
Reset							1	0	1	0						

Bit(s)	Name	Description
9	XO_PTATCTAT_EN_FPM	
8	XO_PTATCTAT_EN_LPM	
7	XO_PTATCTAT_EN_M	
6	XO_PTATCTAT_EN_MAN	

091A **PSC_TOP_INT_STATUS0** **PSC_TOP INT Status Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_INT_STATUS_OV						RG_INT_STATUS_VCDT_HV_DET		RG_INT_STATUS_CHRDET					
Type			W1C						W1C		W1C					
Reset			0						0		0					

Bit(s)	Name	Description
13	RG_INT_STATUS_OV	**OV interrupt status** 0: No interrupt issued 1: Interrupt issued
7	RG_INT_STATUS_VCDT_HV_DET	**VCDT_HV_DET interrupt status** 0: No interrupt issued 1: Interrupt issued
5	RG_INT_STATUS_CHRDET	**CHRDET interrupt status** 0: No interrupt issued 1: Interrupt issued

098A **STRUP_ANA_CON1** **STRUP Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_EN2	RG_EN1	RG_RST						

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

								_DR VSE L	_DR VSE L	_DR VSE L						
Type								RW	RW	RW						
Reset								0	0	0						

Bit(s)	Name	Description
8	RG_EN2_DRVSEL	**Selects EXT_PMIC_EN2 pin output driving capability** 0: 7.5mA (default) 1: 15mA
7	RG_EN1_DRVSEL	**Selects EXT_PMIC_EN1 pin output driving capability** 0: 7.5mA (default) 1: 15mA
6	RG_RST_DRVSEL	**Selects reset pin output driving capability** 0: 7.5mA (default) 1: 15mA

0A08 **PPCCTL0** **PPC Control 0 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_USBDL_MODE				RG_PWRHOLD
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	RG_USBDL_MODE	**Disables BWDT in USBDL mode** 0: Normal mode 1: USBDL mode -> disable BWDT
0	RG_PWRHOLD	**Power hold** 0->1: Power hold 1->0: Power down

0A0E **PPCCFG0** **PPC Configuration 0 Register** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_WDTRST_ACT					
Type											RW					
Reset											0	0				

Bit(s)	Name	Description
5:4	RG_WDTRST_ACT	**PSEQ WDT actions** 00: PMIC reg reset 01: Warm reset 10: Cold reset 11: Reserved

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

0A1C **STRUP_CON4** **STRUP DIG Control Register N4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		JUST_PWRKEY_RST	JUST_SMART_RST													
Type		RO	RO													
Reset		0	0													

Bit(s)	Name	Description
14	JUST_PWRKEY_RST	Long pressed reset indicator
13	JUST_SMART_RST	Smart reset indicator

0A1E **STRUP_CON5** **STRUP DIG Control Register N5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DA_EXT_PMIC_EN2	DA_EXT_PMIC_EN1								
Type							RO	RO								
Reset							0	0								

Bit(s)	Name	Description
9	DA_EXT_PMIC_EN2	**External PMIC power on signal** 0: External PMIC shutdown 1: External PMIC power on
8	DA_EXT_PMIC_EN1	**External PMIC power on signal** 0: External PMIC shutdown 1: External PMIC power on

0A2C **STRUP_CON12** **STRUP DIG Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_STRUP_LONG_PRESS_EXT_EN	RG_STRUP_LONG_PRESS_EXT_TD		RG_STRUP_LONG_PRESS_EXT_SEL	
Type												RW	RW		RW	
Reset												0	0	0	0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
4	RG_STRUP_LONG_PRESS_EXT_EN	**Enables re-power on scenario function** 1'b0: Disable long_press re-power on case 1'b1: Enable long_press re-power on case
3:2	RG_STRUP_LONG_PRESS_EXT_TD	**Selects delay time** 2'b00: 0.5s 2'b01: 1s 2'b10: 2s
1:0	RG_STRUP_LONG_PRESS_EXT_SEL	**Selects re-power-on scenario** 2'b00: Debounce pwrkey 2'b01: After release pwrkey 2'b10: After release pwrkey and press pwrkey again

0A2E **STRUP_CON13** **STRUP DIG Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_STRUP_PWRKEY_COUNT_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_STRUP_PWRKEY_COUNT_RESET	**Resets long press shutdown counter** 1'b0: Not reset long press counter 1'b1: Reset long press counter

0A88 **CHR_TOP_CON0** **Charger Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RGS_CHRDET	RGS_CHR_LDO_DET	RGS_VBAT_OV_DET	RGS_OTG_BVALID_DET	RGS_CHRWDT_OUT
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RGS_CHRDET	**Detects charger-in** 0: No valid charger detected 1: Valid charger detected
3	RGS_CHR_LDO_DET	**Detectsc charger LDO** If not detected, pulse charger cannot work. 0: Invalid charger LDO

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: Valid charger LDO
2	RGS_VBAT_OV_DET	**Detects VBAT_OV voltage** 0: VBAT voltage < VBAT_OV_VTH 1: VBAT voltage > VBAT_OV_VTH
1	RGS_OTG_BVALID_DET	**Indicates if the session for B-peripheral is valid (0.8V < Vth < 4V)** Here VBUS is connected to CHRIN. 0: Vbus < 0.8V 1: Vbus > 4V
0	RGS_CHRWDT_OUT	**Timeout flag for charger watchdog timer** Read: 0: No timeout status 1: Timeout status asserted

0A8C **CHR_TOP_CON2** **Charger Top Control Register 2** **0009**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_UVLO_VTHL					RG_VCDT_UVLO_VTH	RG_VCDT_UVLO_EN
Type										RW					RW	RW
Reset										0	0	0	1	0	0	1

Bit(s)	Name	Description
6:2	RG_UVLO_VTHL	**Selects UVLO low threshold** 00000: 2.5V 00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V
1	RG_VCDT_UVLO_VTH	**Selects VBUS_UVLO threshold** 0: 3.9V (default) 1: 3V
0	RG_VCDT_UVLO_EN	**Enables VBUS_UVLO threshold selection** 0: Disable 1: Enable (default)

0A8E **CHR_TOP_CON3** **Charger Top Control Register 3** **0C4E**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VBAT_OV_VTH			RG_VCDT_HV_VTH					RG_VCDT_LV_VTH					
Type			RW			RW					RW					
Reset			0	0	1	1	0	0	0	1	0	0	1	1	1	

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
13:11	RG_VBAT_OV_VTH	**Battery over-voltage detection threshold** 000: 4.200V 001: 4.200V (default) 010: 4.300V 011: 4.400V 100: 4.450V 101: 4.500V 110: 4.600V 111: 4.700V
10:6	RG_VCDT_HV_VTH	**ChargerIn LV detection threshold** Default: 4.3/10.5V for VTHL/VTHH 00000: 3V (for VBUS_UVLO) 00001: 3.9V (for VBUS_UVLO) 00010~01010: 4.0V, 4.1V~4.45V with 50mV/step 01011~01110: 6V~7.5V with 500mV/step 01111~10011: 8.5 ~12.5 with 1000mV/step 10100: 14V
5:1	RG_VCDT_LV_VTH	**ChargerIn LV detection threshold** Default: 4.3/10.5V for VTHL/VTHH 00000: 3V (for VBUS_UVLO) 00001: 3.9V (for VBUS_UVLO) 00010~01010: 4.0V, 4.1V~4.45V with 50mV/step 01011~01110: 6V~7.5V with 500mV/step 01111~10011: 8.5 ~12.5 with 1000mV/step 10100: 14V

0A92 **CHR_TOP_CON5** **Charger Top Control Register 5** **0005**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_VBAT_CV_VTH				
Type												RW				
Reset												0	0	1	0	1

Bit(s)	Name	Description
4:0	RG_VBAT_CV_VTH	**Battery CV detection threshold trimming option** Default: 4.2V This register is used for FT CV threshold trimming, not for customer's fine-tuning. 00000~000011: 3.9V, 4V, 4.05V, 4.1V 00100~00111: 4.15V, 4.2V (default), 4.2125V, 4.225V 01000~01011: 4.2375V, 4.25V, 4.2625V, 4.275V 01100~01111: 4.2875V, 4.3V, 4.3125V, 4.325V 10000~10011: 4.3375V, 4.35V, 4.3625V, 4.375V 10100~10111: 4.3875V, 4.4V, 4.4125V, 4.425V 11000~11011: 4.4375V, 4.45V,4.4625V, 4.475V 11100~11110: 4.4875V, 4.5V, 4.6V 11111: 2.2V (BC1.1)

0A94 **CHR_TOP_CON6** **Charger Top Control Register 6** **0083**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_			RG_LBAT_INT_VTH				

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									OTG_BVALID_EN							
Type									RW			RW				
Reset									1			0	0	0	1	1

Bit(s)	Name	Description
7	RG_OTG_BVALID_EN	**Enables OTG BValid detection** 0: Disable 1: Enable
4:0	RG_LBAT_INT_VTH	**LBAT_INT threshold voltage** 00000: 2.5V 00001: 2.55V 00010: 2.6V 00011: 2.65V (default) 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V 01001: 2.95V 01010: 3.0V 01011: 3.05V 01100: 3.1V 01101: 3.15V 01110: 3.2V 01111: 3.25V 10000: 3.3V 10001: 3.35V 10010: 3.4V

0B88 CHR_CON0 Charger Control Register 0 0F2F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCDT_HV_EN	RG_VBAT_CC_EN	RG_VBAT_CC_VTH		RG_VBAT_CV_EN	RG_VBAT_OV_DEG	RG_VBAT_OV_EN	RG_CS_EN	RG_CS_VTH			
Type					RW	RW	RW		RW	RW	RW	RW	RW			
Reset					1	1	1	1	0	0	1	0	1	1	1	1

Bit(s)	Name	Description
11	RG_VCDT_HV_EN	**Enables ChargerIn HV detection function** 0: Disable 1: Enable
10	RG_VBAT_CC_EN	**Enables battery CC detection** 0: Disable 1: Enable
9:8	RG_VBAT_CC_VTH	**Battery CC detection threshold** 00: 3.3V 01: 3.35V 10: 3.4V 11: 3.45V (default)
7	RG_VBAT_CV_EN	**Enables battery CV detection**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		0: Disable 1: Enable
6	RG_VBAT_OV_DEG	**Enables VBAT OV voltage detection deglitch** 0: No debounce 1: Debounce one cycle (1us)
5	RG_VBAT_OV_EN	**Battery over-voltage for driving protection** 0: Disable 1: Enable
4	RG_CS_EN	**Enables current sense voltage detection comparator** 0: Disable 1: Enable
3:0	RG_CS_VTH	**Current sense voltage detection threshold @ Rcs=65mohm** 1111: 70mA 1110: 200mA 1101: 300mA 1100: 450mA (usbdl) 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA 0110: 1000mA 0101: 1100mA 0100: 1200mA 0011: 1350mA 0010: 1500mA 0001: 1600mA 0000: 2000mA

0B8A **CHR_CON1** **Charger Control Register 1** **0104**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_CHR_EN	RG_CSDAC_EN	RG_ULC_DET_EN	RG_HWCV_EN	RG_TRACKING_EN	RG_CSDAC_MODE	RG_CV_MODE	RG_LOW_ICH_DB					
Type				RW	RW	RW	RW	RW	RW	RW	RW					
Reset				0	0	0	0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
12	RG_CHR_EN	**Charger enable setting** Will gate RG_CSDAC_MODE, RG_CSDAC_EN and RG_HWCV_EN. 0: Disable charger 1: Enable charger
11	RG_CSDAC_EN	**Enables CS DAC** 0: Disable CS DAC 1: Enable CS DAC
10	RG_ULC_DET_EN	**Enables charger plug out auto detection** This function has to be applied with RG_HWCV_EN=1. 0: Disable 1: Enable
9	RG_HWCV_EN	**Enables hardware CV current tracking** 0: Disable 1: Enable

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
8	RG_TRACKING_EN	0: Current calibration use CS_VTH[n] and CS_VTH[n-1] as high/low threshold. 1: Current calibration use CS_VTH[n] and LTH as high/low threshold.
7	RG_CSDAC_MODE	0: If not entering CC, charging is AUTO mode. 1: If leaving UVLO, charging is controlled by RG_CSDAC_EN (same as CC mode).
6	RG_CV_MODE	**Selects battery CV detection mode** 0: CV detection can only be active in off state. 1: CV detection is active in both on and off state.
5:0	RG_LOW_ICH_DB	**Plug out HW detection debounce time (base=16ms)** Debounce time: Code*16ms

0B8C CHR_CON2 Charger Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RGS_VCDT_HV_DET**	**RGS_VCDT_LV_DET**	**RGS_VBAT_CC_DET**	**RGS_VBAT_CV_DET**	**RGS_CS_DET**
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RGS_VCDT_HV_DET	**Charger-in high voltage detection (with de-bounce)** 0: Charge-in voltage < VCDT_HV_VTH 1: Charge-in voltage > VCDT_HV_VTH
3	RGS_VCDT_LV_DET	**Charger-in low voltage detection (with de-bounce)** 0: Charge-in voltage < VCDT_LV_VTH 1: Charge-in voltage > VCDT_LV_VTH
2	RGS_VBAT_CC_DET	**VBAT voltage detection for CC** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
1	RGS_VBAT_CV_DET	**VBAT voltage detection for CV** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
0	RGS_CS_DET	**Current sense voltage detection** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH

0B8E CHR_CON3 Charger Control Register 3 0494

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**RG_CSDAC_STP**			**RG_CSDAC_DLY**		
Type											RW			RW		
Reset											0	1	0	1	0	0

Bit(s)	Name	Description
5:3	RG_CSDAC_STP	**Current DAC output step timer** 1/1/2/3/4/5/6/7 code/ per-step

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
2:0	RG_CSDAC_DLY	**Current DAC output detection delay control** 16/32/64/128/256/512/1024/2048us (512us default, reuse in HW CV mode)

0B94 CHR_CON6 Charger Control Register 6 02A8

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_DAC_USBDL_MAX										RG_USBDL_SET	RG_USBDL_RST	RG_FRC_CSVTH_USBDL
Type				RW										RW	RW	RW
Reset				0	0	0	1	0	1	0	1	0	1	0	0	0

Bit(s)	Name	Description
12:3	RG_DAC_USBDL_MAX	**USBDL maximum current setting** Default: 85 => 0001010101
2	RG_USBDL_SET	**USBDL_MODE software set control** 0: No effect 1: Force to enter USBDL MODE
1	RG_USBDL_RST	**USBDL_MODE software reset control** 0: No effect 1: Force to leave USBDL MODE (priority is less than USBDL_SET)
0	RG_FRC_CSVTH_USBDL	**Forces CS DAC detection threshold to maximum in USB download mode** 0: CS_VTH=450mA in USBDL mode 1: CS_VTH=1600mA in USBDL mode

0B98 CHR_CON8 Charger Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RGS_BC11_CMP_OUT	RG_BC11_DCD_EN	RG_BC11_VSRC_EN		RG_BC11_RST	RG_BC11_BB_CTRL	RG_BC11_BIAS_EN	RG_BC11_IPU_EN		RG_BC11_IPD_EN		RG_BC11_CMP_EN		RG_BC11_VREF_VTH	
Type		RO	RW	RW		RW	RW	RW	RW		RW		RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RGS_BC11_CMP_OUT	**Comparison result of BC11 charger detection** 0: DP or DM < BC11_VREF_VTH 1: DP or DM > BC11_VREF_VTH
13	RG_BC11_DCD_EN	**BC11 DCD connection check 15k resistor to gnd**
12:11	RG_BC11_VSRC_EN	**BC11 voltage source** Set VDP_SRC = 0.6V 0: Disable the voltage 1: Enable the voltage source to DM 2: Enable the voltage source to DP 3: Forbidden

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
10	RG_BC11_RST	**Resets BC11 detection mechanism in PCHR_DIG** 0: No effect 1: BC11 detection mechanism is disabled in PCHR_DIG.
9	RG_BC11_BB_CTRL	**Forces BC11 charger detection controlled by baseband** 0: BC11 detection by PCHR_DIG (hardware mode) 1: BC11 detection by baseband (software mode)
8	RG_BC11_BIAS_EN	**Enables BC11 detection bias circuit** 0: Disable 1: Enable
7:6	RG_BC11_IPU_EN	**Enables BC11 7~15uA pull up current** 0: Disable the pull-up current 1: Enable the pull-up current to DM 2: Enable the pull-up current to DP 3: Forbidden
5:4	RG_BC11_IPD_EN	**BC11 50~150uA pull down current** 0: Disable the pull-down current 1: Enable the pull-down current to DM 2: Enable the pull-down current to DP 3: Forbidden
3:2	RG_BC11_CMP_EN	**BC11 comparator connection** 0: Disable the comparator 1: Enable the comparator to DM 2: Enable the comparator to DP 3: Forbidden
1:0	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH=0.325V 1: VREF_VTH=1.2V 2,3: VREF_VTH=2.6V (for Apple adaptor)

0B9A **CHR_CON9** **Charger Control Register 9** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CHRWDT_WR	RG_CHRWDT_EN	RG_CHRWDT_TD				RG_ENVTEM_EN	RG_ENVTEM_D
Type									W1	RW	RW				W1	RW
Reset									0	1	0	0	0	0	0	0

Bit(s)	Name	Description
7	RG_CHRWDT_WR	**Resets charger watchdog timer and update CHRWDT_TD** 0: Reset inactive 1: Reset active and CHRWDT_TD updated to PCHR_DIG
6	RG_CHRWDT_EN	**Enables setting for charger watchdog timer** Note: UVLO don't care this bit and will time out after 3000s. PCHR_TESTMODE can force to control watchdog enable by using this bit. 0: Disable 1: Enable if (CHR_EN(@CHR_CON0) == 1)
5:2	RG_CHRWDT_TD	**Time constant setting for charger watchdog timer** 0: 4 sec 1: 8 sec 2: 16 sec 3: 32 sec

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4: 128 sec 5: 256 sec 6: 512 sec 7: 1024 sec 8~15: 3000 sec
1	RG_ENVTEM_EN	**Blocks CHR_DET signal to start_up** 0: N/A 1: Enable write
0	RG_ENVTEM_D	**Blocks CHR_DET signal to start_up** 0: Not block 1: Block

0D12 **FGADC_CAR_CON0** **FGADC_CAR Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_15_00	Current charge value [15:0]

0D14 **FGADC_CAR_CON1** **FGADC_CAR Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_31_16	Current charge value [31:16]

0D16 **FGADC_CAR_CON2** **FGADC_CAR Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FG_CAR_34_32		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	FG_CAR_34_32	Current charge value [34:32]

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

0D20 **FGADC_NTER_CON0** **FGADC_NTER Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_15_00	Current charge time value [15:0]

0D22 **FGADC_NTER_CON1** **FGADC_NTER Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_31_16	Current charge time value [31:16]

0D24 **FGADC_NTER_CON2** **FGADC_NTER Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FG_NTER_32
Type																RO
Reset																0

Bit(s)	Name	Description
0	FG_NTER_32	Current charge time value [32]

0D8A **FGADC_CUR_CON0** **FGADC_CUR Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CURRENT_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CURRENT_OUT	Current output charge of first stage[15:0]

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

0E08 **BATON_ANA_CON0** **BATON Analog Control Register 0** **0005**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**RGS_BATON_HT**	**RG_BATON_HT_VTH**		**RG_BATON_HT_EN**	**RG_BATON_LT_EN**	**RGS_BATON_UNDET**	**RG_BATON_EN**
Type										RO	RW		RW	RW	RO	RW
Reset										0	0	0	0	1	0	1

Bit(s)	Name	Description
6	RGS_BATON_HT	**BATON HT detect Flag**
5:4	RG_BATON_HT_VTH	**Selects BATON HT temperature threshold**
3	RG_BATON_HT_EN	**Battery-on HW HT temperature detection gating** 0: Disable 1: Enable
2	RG_BATON_LT_EN	**Detects battery-on HW low temperature** 0: Disable 1: Enable
1	RGS_BATON_UNDET	**Battery-on undetected** 0: Detected 1: Not detected
0	RG_BATON_EN	**BATON battery detection comparator enable (gated by CHR_LDO_DET to default 1 in analog domain)** 0: Disable 1: Enable (default)

1088 **AUXADC_ADC0** **AUXADC ADC Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH0**	**AUXADC_ADC_OUT_CH0**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

108A **AUXADC_ADC1** **AUXADC ADC Register 1** **0000**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

108A AUXADC_ADC1 AUXADC ADC Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1	AUXADC_ADC_OUT_CH1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

108C AUXADC_ADC2 AUXADC ADC Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH2				AUXADC_ADC_OUT_CH2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH2	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

108E AUXADC_ADC3 AUXADC ADC Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH3				AUXADC_ADC_OUT_CH3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RD	**AUXADC channel 3 output data ready**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	Y_CH3	0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

1090 **AUXADC_ADC4** **AUXADC ADC Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

1092 **AUXADC_ADC5** **AUXADC ADC Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH5				AUXADC_ADC_OUT_CH5											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

1094 **AUXADC_ADC6** **AUXADC ADC Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC				AUXADC_ADC_OUT_CH6											

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

	_ADC_RDY_CH6															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

1096 AUXADC_ADC7 AUXADC ADC Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7	AUXADC_ADC_OUT_CH7														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

1098 AUXADC_ADC8 AUXADC ADC Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH8				AUXADC_ADC_OUT_CH8											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

109A **AUXADC_ADC9** **AUXADC ADC Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH9	AUXADC_ADC_OUT_CH9														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

109C **AUXADC_ADC10** **AUXADC ADC Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH10				AUXADC_ADC_OUT_CH10											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH10	**AUXADC channel 10 output data**

109E **AUXADC_ADC11** **AUXADC ADC Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_R				AUXADC_ADC_OUT_CH11											

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

109E AUXADC_ADC11 AUXADC ADC Register 11 0000

	DY_CH11															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready (used for BIF)** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data (used for BIF)**

10A0 AUXADC_ADC12 AUXADC ADC Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15	AUXADC_ADC_OUT_CH12_15														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

10A2 AUXADC_ADC14 AUXADC ADC Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT				AUXADC_ADC_OUT_LBAT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

10A4 **AUXADC_ADC16** **AUXADC ADC Register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_GPS	AUXADC_ADC_OUT_CH7_BY_GPS														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_GPS	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_GPS	**AUXADC channel 7 output data**

10A6 **AUXADC_ADC17** **AUXADC ADC Register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_MD	AUXADC_ADC_OUT_CH7_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_MD	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_MD	**AUXADC channel 7 output data**

10A8 **AUXADC_ADC18** **AUXADC ADC Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

10A8 AUXADC_ADC18 AUXADC ADC Register 18 0000

Name	**AUXADC_ADC_RDY_CH7_BY_AP**	**AUXADC_ADC_OUT_CH7_BY_AP**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_AP	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_AP	**AUXADC channel 7 output data**

10AA AUXADC_ADC19 AUXADC ADC Register 19 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH4_BY_MD**				**AUXADC_ADC_OUT_CH4_BY_MD**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_MD	**AUXADC channel 4 output data**

10AC AUXADC_ADC20 AUXADC ADC Register 20 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_PWRON_PCHR**	**AUXADC_ADC_OUT_PWRON_PCHR**														
Type	RO	RO														

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

10AC	AUXADC_ADC20	AUXADC ADC Register 20	0000

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_PWRON_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_PWRON_PCHR	**AUXADC wakeup output data**

10AE	AUXADC_ADC21	AUXADC ADC Register 21	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_PWRON_SWCHR	AUXADC_ADC_OUT_PWRON_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_PWRON_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_PWRON_SWCHR	**AUXADC wakeup output data**

10B0	AUXADC_ADC22	AUXADC ADC Register 22	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

10B2 **AUXADC_ADC23** **AUXADC ADC Register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_SWCHR	AUXADC_ADC_OUT_WAKEUP_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

10B4 **AUXADC_ADC24** **AUXADC ADC Register 24** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_MD	AUXADC_ADC_OUT_CH0_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_MD	**AUXADC channel output data**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

10B6 **AUXADC_ADC25** **AUXADC ADC Register 25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_AP	AUXADC_ADC_OUT_CH0_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_AP	**AUXADC channel output data**

10B8 **AUXADC_ADC26** **AUXADC ADC Register 26** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_MD	AUXADC_ADC_OUT_CH1_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_MD	**AUXADC channel output data**

10BA **AUXADC_ADC27** **AUXADC ADC Register 27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_AP	AUXADC_ADC_OUT_CH1_BY_AP														
Type	RO	RO														

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_AP	**AUXADC channel output data**

10BC **AUXADC_ADC29** **AUXADC ADC Register 29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC_PCHR	AUXADC_ADC_OUT_FGADC_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC_PCHR	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC_PCHR	**AUXADC output data**

10BE **AUXADC_ADC30** **AUXADC ADC Register 30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC_SWCHR	AUXADC_ADC_OUT_FGADC_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC_SWCHR	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC_SWCHR	**AUXADC output data**

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

10C0	AUXADC_ADC31	AUXADC ADC Register 31	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_PLUGIN_PCHR	AUXADC_ADC_OUT_BAT_PLUGIN_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_PLUGIN_PCHR	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_BAT_PLUGIN_PCHR	**AUXADC output data**

10C2	AUXADC_ADC32	AUXADC ADC Register 32	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_PLUGIN_SWCHR	AUXADC_ADC_OUT_BAT_PLUGIN_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_PLUGIN_SWCHR	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_BAT_PLUGIN_SWCHR	**AUXADC output data**

10C4	AUXADC_ADC33	AUXADC ADC Register 33	0000

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

10C4 **AUXADC_ADC33** **AUXADC ADC Register 33** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP	AUXADC_ADC_OUT_IMP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP	**AUXADC output data**

10C6 **AUXADC_ADC34** **AUXADC ADC Register 34** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP_AVG	AUXADC_ADC_OUT_IMP_AVG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP_AVG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP_AVG	**AUXADC output data**

10C8 **AUXADC_ADC35** **AUXADC ADC Register 35** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	AUXADC channel output raw data

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

10CA	AUXADC_ADC36	AUXADC ADC Register 36	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDRT	AUXADC_ADC_OUT_MDRT														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDRT	**AUXADC output data**

10D4	AUXADC_ADC42	AUXADC ADC Register 42	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_NAG	AUXADC_ADC_OUT_NAG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_NAG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_NAG	**AUXADC output data**

10D6	AUXADC_ADC43	AUXADC ADC Register 43	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BATID				AUXADC_ADC_OUT_BATID											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BATID	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_BATID	**AUXADC output data**

10D8 **AUXADC_ADC46** **AUXADC ADC Register 46** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_THR1				AUXADC_ADC_OUT_CH4_BY_THR1											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_THR1	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_THR1	**AUXADC channel 4 output data**

10DA **AUXADC_ADC47** **AUXADC ADC Register 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_THR2				AUXADC_ADC_OUT_CH4_BY_THR2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_THR2	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_THR2	**AUXADC channel 4 output data**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1108	AUXADC_STA0	AUXADC_STA0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_WAKEUP			AUXADC_ADC_BUSY_IN_LBAT	AUXADC_ADC_BUSY_IN											
Type	RO			RO	RO											
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 0: Idle 1: Busy
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 0: Idle 1: Busy
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC BUSY STATUS, bit[11] = CH11 ~ bit[0] = CH0** 0: Idle 1: Busy

110A	AUXADC_STA1	AUXADC_STA1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_THR_MD		AUXADC_ADC_BUSY_IN_GPS	AUXADC_ADC_BUSY_IN_GPS_MD	AUXADC_ADC_BUSY_IN_GPS_AP	AUXADC_ADC_BUSY_IN_FGADC_SWCHR	AUXADC_ADC_BUSY_IN_FGADC_PCHR	AUXADC_ADC_BUSY_IN_IMP	AUXADC_ADC_BUSY_IN_SHARE							
Type	RO		RO	RO	RO	RO	RO	RO	RO							
Reset	0		0	0	0	0	0	0	0							

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_THR_MD	**ADC busy status** 0: Idle 1: Busy
13	AUXADC_ADC_BUSY_IN_GPS	**ADC busy status** 0: Idle 1: Busy
12	AUXADC_ADC_BUSY_IN_GPS_MD	**ADC busy status** 0: Idle 1: Busy
11	AUXADC_ADC_BUSY_IN_GPS_AP	**ADC busy status** 0: Idle

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: Busy
10	AUXADC_ADC_BUSY_IN_FGADC_SWCHR	**ADC busy status** 0: Idle 1: Busy
9	AUXADC_ADC_BUSY_IN_FGADC_PCHR	**ADC busy status** 0: Idle 1: Busy
8	AUXADC_ADC_BUSY_IN_IMP	**ADC busy status** 0: Idle 1: Busy
7	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 0: Idle 1: Busy

110C **AUXADC_STA2** **AUXADC_STA2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_BUSY_IN_NAG**			**AUXADC_ADC_BUSY_IN_THR2**	**AUXADC_ADC_BUSY_IN_THR1**								**AUXADC_ADC_BUSY_IN_PWRON**	**AUXADC_ADC_BUSY_IN_BATID**	**AUXADC_ADC_BUSY_IN_BAT_PLUGIN_SWCHR**	**AUXADC_ADC_BUSY_IN_BAT_PLUGIN_PCHR**
Type	RO			RO	RO								RO	RO	RO	RO
Reset	0			0	0								0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_NAG	**ADC busy status** 0: Idle 1: Busy
12	AUXADC_ADC_BUSY_IN_THR2	**ADC busy status** 0: Idle 1: Busy
11	AUXADC_ADC_BUSY_IN_THR1	**ADC busy status** 0: Idle 1: Busy
3	AUXADC_ADC_BUSY_IN_PWRON	**ADC busy status** 0: Idle 1: Busy
2	AUXADC_ADC_BUSY_IN_BATID	**ADC busy status** 0: Idle 1: Busy
1	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_SWCHR	**ADC busy status** 0: Idle 1: Busy
0	AUXADC_ADC_BUSY_IN_BAT_PLUGI	**ADC busy status**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	N_PCHR	0: Idle 1: Busy

140C **BUCK_TOP_CLK_CON0** **BUCK_TOP Clock Control 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BUCK_ANA_CK_PDN				
Type												RW				
Reset												0				

Bit(s)	Name	Description
4	RG_BUCK_ANA_CK_PDN	**Powers down BUCK_ANA_CK** 0: Power on 1: Power down

1434 **BUCK_TOP_OC_CON0** **BUCK_TOP OC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BUCK_VPA_OC_SDN_STATUS	RG_BUCK_VS1_OC_SDN_STATUS	RG_BUCK_VMODEM_OC_SDN_STATUS	RG_BUCK_VCORE_OC_SDN_STATUS	RG_BUCK_VPROC_OC_SDN_STATUS
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RG_BUCK_VPA_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
3	RG_BUCK_VS1_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
2	RG_BUCK_VMODEM_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
1	RG_BUCK_VCORE_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
0	RG_BUCK_VPROC_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: OC occurs.

1488 **BUCK_VPROC_CON0** **BUCK VPROC Control 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VPROC_LP	RG_BUCK_VPROC_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VPROC_LP	**Enter low power mode** Valid once RG_BUCK_VPROC_SW_OP_EN = 1'b1 0: No LP 1: LP
0	RG_BUCK_VPROC_EN	**Enable control (SW mode)** Valid once RG_BUCK_VPROC_SW_OP_EN = 1'b1 0: Off 1: On

148A **BUCK_VPROC_CON1** **BUCK VPROC Control 1** **007F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC_VOSEL_SLEEP						
Type										RW						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC_VOSEL_SLEEP	**VOUT selection in sleep mode** Give the same voltage as RG_VPROC_VSLEEP_SEL Vout = 0.51875V + 6.25mV*code

14AA **BUCK_VPROC_ELR0** **BUCK_VPROC ELR 0 Register** **007F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC_VOSEL						
Type										RW						
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC_VOSEL	**VOUT selection in normal mode (SW mode)** Vout = 0.51875V + 6.25mV*code

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1508	BUCK_VCORE_CON0	BUCK VCORE Control 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VCORE_LP	RG_BUCK_VCORE_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VCORE_LP	**Enter low power mode** Valid once RG_BUCK_VCORE_SW_OP_EN = 1'b1 0: No LP 1: LP
0	RG_BUCK_VCORE_EN	**Enable control (SW mode)** Valid once RG_BUCK_VCORE_SW_OP_EN = 1'b1 0: Off 1: On

150A	BUCK_VCORE_CON1	BUCK VCORE Control 1	005C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VCORE_VOSEL_SLEEP						
Type										RW						
Reset										1	0	1	1	1	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VCORE_VOSEL_SLEEP	**VOUT selection in sleep mode** Give the same voltage as RG_VCORE_VSLEEP_SEL Vout = 0.51875V + 6.25mV*code

152A	BUCK_VCORE_ELR0	BUCK_VCORE ELR 0 Register	005C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VCORE_VOSEL						
Type										RW						
Reset										1	0	1	1	1	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VCORE_VOSEL	**VOUT selection in normal mode (SW mode)** Vout = 0.51875V + 6.25mV*code

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1588 BUCK_VMODEM_CON0 BUCK VMODEM Control 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VMODEM_LP	RG_BUCK_VMODEM_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VMODEM_LP	**Enter low power mode** Valid once RG_BUCK_VMODEM_SW_OP_EN = 1'b1 0: No LP 1: LP
0	RG_BUCK_VMODEM_EN	**Enable control (SW mode)** Valid once RG_BUCK_VMODEM_SW_OP_EN = 1'b1 0: Off 1: On

158A BUCK_VMODEM_CON1 BUCK VMODEM Control 1 0068

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VMODEM_VOSEL_SLEEP						
Type										RW						
Reset										1	1	0	1	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VMODEM_VOSEL_SLEEP	**VOUT selection in sleep mode** Give the same voltage as RG_VMODEM_VSLEEP_SEL Vout = 0.5V + 6.25mV*code

15AA BUCK_VMODEM_ELR0 BUCK_VMODEM ELR 0 Register 0068

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VMODEM_VOSEL						
Type										RW						
Reset										1	1	0	1	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VMODEM_VOSEL	**VOUT selection in normal mode (SW mode)** Vout = 0.5V + 6.25mV*code

1608 BUCK_VS1_CON0 BUCK VS1 Control 0 0001

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1608 BUCK_VS1_CON0 BUCK VS1 Control 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VS1_LP	RG_BUCK_VS1_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VS1_LP	**Enter low power mode** Valid once RG_BUCK_VS1_SW_OP_EN = 1'b1 0: No LP 1: LP
0	RG_BUCK_VS1_EN	**Enable control (SW mode)** Valid once RG_BUCK_VS1_SW_OP_EN = 1'b1 0: OFF 1: ON

160A BUCK_VS1_CON1 BUCK VS1 Control 1 0048

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VS1_VOSEL_SLEEP						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VS1_VOSEL_SLEEP	**VOUT selection in sleep mode** Give the same voltage as RG_VS1_VSLEEP_SEL. VOUT = 2*(0.6V + 6.25mV*VOSEL)

1632 BUCK_VS1_ELR0 BUCK_VS1 ELR 0 Register 0048

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VS1_VOSEL						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VS1_VOSEL	**VOUT selection in normal mode (SW mode)** VOUT = 2*(0.6V + 6.25mV*VOSEL)

1688 BUCK_VPA_CON0 BUCK VPA Control 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1688 BUCK_VPA_CON0 BUCK VPA Control 0 0000

Name																RG_BUCK_VPA_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_BUCK_VPA_EN	Enable control (SW mode)

168A BUCK_VPA_CON1 BUCK VPA Control 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BUCK_VPA_VOSEL					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	RG_BUCK_VPA_VOSEL	**VOUT selection in normal mode (SW mode)** VOUT = 0.5V + 50mV*VOSEL

170A SMPS_ANA_CON1 SMPS Control Register 1 0140

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VMODEM_SLEEP_VOLTAGE			RG_VCORE_SLEEP_VOLTAGE							
Type						RW			RW							
Reset						0	0	1	0	1	0					

Bit(s)	Name	Description
10:8	RG_VMODEM_SLEEP_VOLTAGE	**Selects sleep mode voltage** 000: 0.5V 001: 0.55V 010: 0.6V 011: 0.75V 100: 0.8V 101: 0.85V 110: 0.7V 111: 0.775V
7:5	RG_VCORE_SLEEP_VOLTAGE	**Selects sleep mode voltage** 000: 0.575V 001: 0.55V 010: 0.625V 011: 0.75V 100: 0.8V 101: 0.85V 110: 0.65V

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		111: 0.775V

170C **SMPS_ANA_CON2** **SMPS Control Register 2** **0292**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_VPROC_SLEEP_VOLTAGE		
Type														RW		
Reset														0	1	0

Bit(s)	Name	Description
2:0	RG_VPROC_SLEEP_VOLTAGE	**Selects sleep mode voltage** 000: 0.5V 001: 0.55V 010: 0.6V 011: 0.75V 100: 0.8V 101: 0.85V 110: 0.7V 111: 0.775V

170E **VCORE_VPROC_ANA_CON0** **VCORE_VPROC Control Register 0** **0018**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_VPROC_FPWM	RG_VCORE_FPWM	
Type														RW	RW	
Reset														0	0	

Bit(s)	Name	Description
2	RG_VPROC_FPWM	1'b0: Auto mode 1'b1: Force PWM mode
1	RG_VCORE_FPWM	1'b0: Auto mode 1'b1: Force PWM mode

1718 **VCORE_VPROC_ANA_CON5** **VCORE_VPROC Control Register 5** **0006**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RGS_VCORE_PREOC_ST	RGS_VPROC_OC_STATU	RGS_VCORE_OC_STATU			

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

											ATUS	S	S			
Type											RO	RO	RO			
Reset											0	0	0			

Bit(s)	Name	Description
5	RGS_VCORE_PREOC_STATUS	**preoc status register** 0: No OC 1: preoc trigger
4	RGS_VPROC_OC_STATUS	**OC status** H: OC L: Normal operation
3	RGS_VCORE_OC_STATUS	**OC status** H: OC L: Normal operation

174C   SMPS_ELR_0   SMPS ELR 0 Register   0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VS1_SLEEP_VOLTAGE														
Type		RW														
Reset		0	0													

Bit(s)	Name	Description
14:13	RG_VS1_SLEEP_VOLTAGE	**Selects sleep mode voltage** 00: 0.93125V (Vout=1.8625V) (default) 01: 0.95V (Vout=1.9V) 10: 0.975V (Vout=1.95V) 11: 1V (Vout=2V)

188C   LDO_TOP_CLK_DCM_CON0   LDO DCM Control Register 0   0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_DCM_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_LDO_DCM_MODE	**LDO 1M/9M CG constraint mode** 1'b0: Old mode 1'b1: New mode (higher gated rate)

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

188E	LDO_TOP_CLK_VIO28_CON0	LDO VIO28 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VIO28_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VIO28_CK_SW_MODE	**VIO28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

1890	LDO_TOP_CLK_VIO18_CON0	LDO VIO18 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VIO18_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VIO18_CK_SW_MODE	**VIO18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

1892	LDO_TOP_CLK_VAUD28_CON0	LDO VAUD28 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VAUD28_CK_SW_MODE
Type																RW

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Reset																1

Bit(s)	Name	Description
0	RG_LDO_VAUD28_CK_SW_MODE	**VAUD28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

1894	LDO_TOP_CLK_VDRAM_CON0	LDO VDRAM Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VDRAM_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VDRAM_CK_SW_MODE	**VDRAM clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

1896	LDO_TOP_CLK_VSRAM_PROC_CON0	LDO VSRAM_PROC Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSRAM_PROC_OSC_SEL_DIS		RG_LDO_VSRAM_PROC_CK_SW_MODE
Type														RW		RW
Reset														0		1

Bit(s)	Name	Description
2	RG_LDO_VSRAM_PROC_OSC_SEL_DIS	**Disables VSRAM_PROC OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
0	RG_LDO_VSRAM_PROC_CK_SW_MODE	**VSRAM_PROC clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1898	LDO_TOP_CLK_VSRAM_OTHERS_CON0	LDO VSRAM_OTHERS Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_LDO_VSRAM_OTHERS_OSC_SEL_DIS		RG_LDO_VSRAM_OTHERS_CK_SW_MODE
Type														RW		RW
Reset														0		1

Bit(s)	Name	Description
2	RG_LDO_VSRAM_OTHERS_OSC_SEL_DIS	**Disables VSRAM_OTHERS OSC_SEL HW mode to CLKCTL** 1'b0: Enable 1'b1: Disable
0	RG_LDO_VSRAM_OTHERS_CK_SW_MODE	**VSRAM_OTHERS clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

189A	LDO_TOP_CLK_VAUX18_CON0	LDO VAUX18 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VAUX18_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VAUX18_CK_SW_MODE	**VAUX18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

189C	LDO_TOP_CLK_VUSB33_CON0	LDO VUSB33 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VUSB33_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VUSB33_CK_SW_MODE	**VUSB33 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

189E	LDO_TOP_CLK_VEMC_CON0	LDO VEMC Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VEMC_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VEMC_CK_SW_MODE	**VEMC clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18A0	LDO_TOP_CLK_VXO22_CON0	LDO VXO22 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VXO22_CK_SW_MODE
Type																RW

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Reset																1

Bit(s)	Name	Description
0	RG_LDO_VXO22_CK_SW_MODE	**VXO22 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18A2 **LDO_TOP_CLK_VSIM1_CON0** **LDO VSIM1 Clock Gating Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VSIM1_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VSIM1_CK_SW_MODE	**VSIM1 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18A4 **LDO_TOP_CLK_VSIM2_CON0** **LDO VSIM2 Clock Gating Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VSIM2_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VSIM2_CK_SW_MODE	**VSIM2 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

18A6	LDO_TOP_CLK_VCAMD_CON0	LDO VCAMD Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMD_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMD_CK_SW_MODE	**VCAMD clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18A8	LDO_TOP_CLK_VCAMIO_CON0	LDO VCAMIO Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMIO_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMIO_CK_SW_MODE	**VCAMIO clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18AA	LDO_TOP_CLK_VEFUSE_CON0	LDO VEFUSE Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VEFUSE_CK_SW_MODE

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VEFUSE_CK_SW_MODE	**VEFUSE clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18AC	LDO_TOP_CLK_VCN33_CON0	LDO VCN33 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN33_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN33_CK_SW_MODE	**VCN33 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18AE	LDO_TOP_CLK_VCN18_CON0	LDO VCN18 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN18_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN18_CK_SW_MODE	**VCN18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

18B0	LDO_TOP_CLK_VCN28_CON0	LDO VCN28 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN28_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN28_CK_SW_MODE	**VCN28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18B2	LDO_TOP_CLK_VIBR_CON0	LDO VIBR Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VIBR_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VIBR_CK_SW_MODE	**VIBR clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18B4	LDO_TOP_CLK_VFE28_CON0	LDO VFE28 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VFE28_CK_SW_MODE
Type																RW
Reset																1

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_LDO_VFE28_CK_SW_MODE	**VFE28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18B6 **LDO_TOP_CLK_VMCH_CON0** **LDO VMCH Clock Gating Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VMCH_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMCH_CK_SW_MODE	**VMCH clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18B8 **LDO_TOP_CLK_VMC_CON0** **LDO VMC Clock Gating Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VMC_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMC_CK_SW_MODE	**VMC clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18BA **LDO_TOP_CLK_VRF18_CON0** **LDO VRF18 Clock Gating Control Register 0** **0001**

 © 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF18_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VRF18_CK_SW_MODE	**VRF18 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18BC	LDO_TOP_CLK_VLDO28_CON0	LDO VLDO28 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VLDO28_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VLDO28_CK_SW_MODE	**VLDO28 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18BE	LDO_TOP_CLK_VRF12_CON0	LDO VRF12 Clock Gating Control Register 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF12_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_LDO_VRF12_CK_SW_MODE	**VRF12 clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18C0 **LDO_TOP_CLK_VCAMA_CON0** **LDO VCAMA Clock Gating Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMA_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMA_CK_SW_MODE	**VCAMA clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

18C2 **LDO_TOP_CLK_TREF_CON0** **LDO TREF Clock Gating Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_TREF_CK_SW_MODE
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_TREF_CK_SW_MODE	**TREF clock DCM mode** 1'b0: HW DCM mode 1'b1: SW mode

1916 **LDO_VXO22_CON1** **LDO VXO22 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VXO							DA_VXO								

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	22_EN							22_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VXO22_EN	**VXO22 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VXO22_MODE	**VXO22 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

192A LDO_VAUX18_CON1 LDO VAUX18 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VAUX18_EN							DA_VAUX18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VAUX18_EN	**VAUX18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VAUX18_MODE	**VAUX18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

193E LDO_VAUD28_CON1 LDO VAUD28 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VAUD28_EN															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_VAUD28_EN	**VAUD28 enable status** 1'b0: Disable 1'b1: Enable

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1952	LDO_VIO28_CON1	LDO VIO28 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VIO28_EN															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_VIO28_EN	**VIO28 enable status** 1'b0: Disable 1'b1: Enable

1966	LDO_VIO18_CON1	LDO VIO18 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VIO18_EN															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_VIO18_EN	**VIO18 enable status** 1'b0: Disable 1'b1: Enable

197A	LDO_VDRAM_CON1	LDO VDRAM Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VDRAM_EN															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_VDRAM_EN	**VDRAM enable status** 1'b0: Disable 1'b1: Enable

1996	LDO_VEMC_CON1	LDO VEMC Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Name	**DA_VEMC_EN**															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_VEMC_EN	**VEMC enable status** 1'b0: Disable 1'b1: Enable

19AC **LDO_VUSB33_CON1** **LDO VUSB33 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_VUSB33_EN**															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_VUSB33_EN	**VUSB33 enable status** 1'b0: Disable 1'b1: Enable

19CE **LDO_VSRAM_PROC_DBG1** **LDO VSRAM_PROC Debug 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DA_VSRAM_PROC_EN**
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_VSRAM_PROC_EN	VSRAM_PROC enable status

19EC **LDO_VSRAM_OTHERS_DBG1** **LDO VSRAM_OTHERS Debug 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DA_**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

																VSRAM_OTHERS_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_VSRAM_OTHERS_EN	VSRAM_OTHERS enable status

1A08 **LDO_VFE28_CON0** **LDO VFE28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VFE28_LP	RG_LDO_VFE28_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VFE28_LP	**Enters low power mode** Valid once RG_LDO_VFE28_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VFE28_EN	**Enable control (SW mode)** Valid once RG_LDO_VFE28_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A0A **LDO_VFE28_OP_EN** **LDO VFE28 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VFE28_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VFE28_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1A16 **LDO_VFE28_CON1** **LDO VFE28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VFE28_EN							DA_VFE28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VFE28_EN	**VFE28 enable status** 1'b1: enable 1'b0: disable
8	DA_VFE28_MODE	**VFE28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1A1C **LDO_VRF18_CON0** **LDO VRF18 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF18_LP	RG_LDO_VRF18_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF18_LP	**Enter low power mode** Valid once RG_LDO_VRF18_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF18_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF18_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A1E **LDO_VRF18_OP_EN** **LDO VRF18 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF18_SW_OP_EN
Type																RW
Reset																1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_LDO_VRF18_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1A2A **LDO_VRF18_CON1** **LDO VRF18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VRF18_EN							DA_VRF18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VRF18_EN	**VRF18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VRF18_MODE	**VRF18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1A30 **LDO_VRF12_CON0** **LDO VRF12 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF12_LP	RG_LDO_VRF12_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF12_LP	**Enter low power mode** Valid once RG_LDO_VRF12_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF12_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF12_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A32 **LDO_VRF12_OP_EN** **LDO VRF12 Operation Enable** **0001**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF12_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VRF12_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1A3E **LDO_VRF12_CON1** **LDO VRF12 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VRF12_EN							DA_VRF12_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VRF12_EN	**VRF12 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VRF12_MODE	**VRF12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1A44 **LDO_VEFUSE_CON0** **LDO VEFUSE Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VEFUSE_LP	RG_LDO_VEFUSE_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VEFUSE_LP	**Enter low power mode** Valid once RG_LDO_VEFUSE_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_LDO_VEFUSE_EN	**Enable control (SW mode)** Valid once RG_LDO_VEFUSE_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A46 LDO_VEFUSE_OP_EN LDO VEFUSE Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VEFUSE_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VEFUSE_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1A52 LDO_VEFUSE_CON1 LDO VEFUSE Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VEFUSE_EN							DA_VEFUSE_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VEFUSE_EN	**VEFUSE enable status** 1'b0: Disable 1'b1: Enable
8	DA_VEFUSE_MODE	**VEFUSE low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1A58 LDO_VCN18_CON0 LDO VCN18 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VC	RG_LDO_VC

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

															N18_LP	N18_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN18_LP	**Enter low power mode** Valid once RG_LDO_VCN18_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN18_EN	**Enable control (SW mode)** Valid once RG_LDO_VCN18_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A5A **LDO_VCN18_OP_EN** **LDO VCN18 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN18_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN18_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1A66 **LDO_VCN18_CON1** **LDO VCN18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCN18_EN							DA_VCN18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCN18_EN	**VCN18 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCN18_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1A6C LDO_VCAMA_CON0 LDO VCAMA Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMA_LP	RG_LDO_VCAMA_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMA_LP	**Enter low power mode** Valid once RG_LDO_VCAMA_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMA_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMA_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A6E LDO_VCAMA_OP_EN LDO VCAMA Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMA_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMA_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1A7A LDO_VCAMA_CON1 LDO VCAMA Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCAMA_EN							DA_VCAMA_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15	DA_VCAMA_EN	**VCAMA enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCAMA_MODE	**VCAMA low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1A88 LDO_VCAMD_CON0 LDO VCAMD Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMD_LP	RG_LDO_VCAMD_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMD_LP	**Enter low power mode** Valid once RG_LDO_VCAMD_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMD_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMD_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A8A LDO_VCAMD_OP_EN LDO VCAMD Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMD_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMD_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1A96 LDO_VCAMD_CON1 LDO VCAMD Control Register 1 0200

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCAMD_EN							DA_VCAMD_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCAMD_EN	**VCAMD enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCAMD_MODE	**VCAMD low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1A9C **LDO_VCAMIO_CON0** **LDO VCAMIO Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMIO_LP	RG_LDO_VCAMIO_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMIO_LP	**Enter low power mode** Valid once RG_LDO_VCAMIO_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMIO_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMIO_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1A9E **LDO_VCAMIO_OP_EN** **LDO VCAMIO Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMIO_SW_OP_EN
Type																RW
Reset																1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_LDO_VCAMIO_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1AAA	LDO_VCAMIO_CON1	LDO VCAMIO Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCAMIO_EN							DA_VCAMIO_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCAMIO_EN	**VCAMIO enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCAMIO_MODE	**VCAMIO low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1AB0	LDO_VMC_CON0	LDO VMC Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMC_LP	RG_LDO_VMC_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMC_LP	**Enter low power mode** Valid once RG_LDO_VMC_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VMC_EN	**Enable control (SW mode)** Valid once RG_LDO_VMC_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1AB2	LDO_VMC_OP_EN	LDO VMC Operation Enable	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

																LDO_VMC_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMC_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1ABE **LDO_VMC_CON1** **LDO VMC Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VMC_EN							DA_VMC_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VMC_EN	**VMC enable status** 1'b0: Disable 1'b1: Enable
8	DA_VMC_MODE	**VMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1AC4 **LDO_VMCH_CON0** **LDO VMCH Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMCH_LP	RG_LDO_VMCH_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMCH_LP	**Enter low power mode** Valid once RG_LDO_VMCH_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VMCH_EN	**Enable control (SW mode)** Valid once RG_LDO_VMCH_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1AC6 **LDO_VMCH_OP_EN** **LDO VMCH Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VMCH_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMCH_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1AD2 **LDO_VMCH_CON1** **LDO VMCH Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VMCH_EN							DA_VMCH_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VMCH_EN	**VMCH enable status** 1'b0: Disable 1'b1: Enable
8	DA_VMCH_MODE	**VMCH low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1AD8 **LDO_VSIM1_CON0** **LDO VSIM1 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VSIM1_LP	RG_LDO_VSIM1_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
1	RG_LDO_VSIM1_LP	**Enter low power mode** Valid once RG_LDO_VSIM1_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VSIM1_EN	**Enable control (SW mode)** Valid once RG_LDO_VSIM1_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1ADA **LDO_VSIM1_OP_EN** **LDO VSIM1 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VSIM1_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VSIM1_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1AE6 **LDO_VSIM1_CON1** **LDO VSIM1 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VSIM1_EN							DA_VSIM1_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VSIM1_EN	**VSIM1 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VSIM1_MODE	**VSIM1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1AEC **LDO_VSIM2_CON0** **LDO VSIM2 Control Register 0** **0000**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VSIM2_LP	RG_LDO_VSIM2_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VSIM2_LP	**Enter low power mode** Valid once RG_LDO_VSIM2_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VSIM2_EN	**Enable control (SW mode)** Valid once RG_LDO_VSIM2_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1AEE LDO_VSIM2_OP_EN LDO VSIM2 Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VSIM2_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VSIM2_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1AFA LDO_VSIM2_CON1 LDO VSIM2 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VSIM2_EN							DA_VSIM2_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VSIM2_EN	**VSIM2 enable status** 1'b0: Disable 1'b1: Enable

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
8	DA_VSIM2_MODE	**VSIM2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1B08 **LDO_VIBR_CON0** **LDO VIBR Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_LDO_VIBR_LP**	**RG_LDO_VIBR_EN**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VIBR_LP	**Enter low power mode** Valid once RG_LDO_VIBR_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VIBR_EN	**Enable control (SW mode)** Valid once RG_LDO_VIBR_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1B0A **LDO_VIBR_OP_EN** **LDO VIBR Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_LDO_VIBR_SW_OP_EN**
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VIBR_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1B16 **LDO_VIBR_CON1** **LDO VIBR Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_VIBR_E**							**DA_VIBR_M**								

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

	N							ODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VIBR_EN	**VIBR enable status** 1'b0: Disable 1'b1: Enable
8	DA_VIBR_MODE	**VIBR low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1B1C **LDO_VCN33_CON0_0** **LDO VCN33 bt Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN33_LP	RG_LDO_VCN33_EN_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN33_LP	**Enter low power mode** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN33_EN_0	**Enable control (SW mode)(BT)** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1B1E **LDO_VCN33_OP_EN** **LDO VCN33 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN33_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN33_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1B2A **LDO_VCN33_CON0_1** **LDO VCN33 wifi Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN33_EN_1
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_LDO_VCN33_EN_1	**Enable control (SW mode)(WIFI)** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1B2C **LDO_VCN33_CON1** **LDO VCN33 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCN33_EN							DA_VCN33_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCN33_EN	**VCN33 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCN33_MODE	**VCN33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1B32 **LDO_VLDO28_CON0_0** **LDO VLDO28 AF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VLDO28_LP	RG_LDO_VLDO28_EN_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
1	RG_LDO_VLDO28_LP	**Enter low power mode** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VLDO28_EN_0	**Enable control (SW mode)(AF)** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1B34 **LDO_VLDO28_OP_EN** **LDO VLDO28 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VLDO28_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VLDO28_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1B40 **LDO_VLDO28_CON0_1** **LDO VLDO28 TP Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VLDO28_EN_1
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_LDO_VLDO28_EN_1	**Enable control (SW mode)(TP)** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1B42 **LDO_VLDO28_CON1** **LDO VLDO28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Name	**DA_VLDO28_EN**							**DA_VLDO28_MODE**								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VLDO28_EN	**VLDO28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VLDO28_MODE	**VLDO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1B88 LDO_VCN28_CON0 LDO VCN28 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_LDO_VCN28_LP**	**RG_LDO_VCN28_EN**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN28_LP	**Enter low power mode** Valid once RG_LDO_VCN28_SW_OP_EN = 1'b1 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN28_EN	**Enable control (SW mode)** Valid once RG_LDO_VCN28_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1B8A LDO_VCN28_OP_EN LDO VCN28 Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_LDO_VCN28_SW_OP_EN**
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN28_S	**Enables SW operation**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	W_OP_EN	1'b0: Disable 1'b1: Enable

1B96 **LDO_VCN28_CON1** **LDO VCN28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VCN28_EN							DA_VCN28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_VCN28_EN	**VCN28 enable status** 1'b0: Disable 1'b1: Enable
8	DA_VCN28_MODE	**VCN28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1B9C **VRTC_CON0** **VRTC Control Register 0** **8002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_VRTC_EN														RG_VRTC_EN	
Type	RO														RW	
Reset	1														1	

Bit(s)	Name	Description
15	DA_VRTC_EN	**VRTC enable status**
1	RG_VRTC_EN	**Enables VRTC** 1'b0: Disable 1'b1: Enable

1B9E **LDO_TREF_CON0** **LDO TREF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_TREF_EN
Type																RW
Reset																0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
0	RG_LDO_TREF_EN	**Enable control (SW mode)** Valid once RG_LDO_TREF_SW_OP_EN = 1'b1 1'b0: Off 1'b1: On

1BA0 LDO_TREF_OP_EN LDO TREF Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_TREF_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_TREF_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1BAC LDO_TREF_CON1 LDO TREF Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_TREF_EN															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_TREF_EN	**TREF enable status** 1'b0: Disable 1'b1: Enable

1C08 VFE28_ANA_CON0 VFE28 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VFE28_VOCAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VFE28_VOCAL	**Calibrates output voltage**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C0C **VCN28_ANA_CON0** **VCN28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VCN28_VOCAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VCN28_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C1C **VCN33_ANA_CON0** **VCN33 Control Register 0** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_VCN33_VOSEL						RG_VCN33_VOCAL			
Type							RW						RW			
Reset							1	1					0	0	0	0

Bit(s)	Name	Description
9:8	RG_VCN33_VOSEL	**Selects output voltage** 2'b01: 3.3V 2'b10: 3.4V 2'b11: 3.5V
3:0	RG_VCN33_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C24 **VLDO28_ANA_CON0** **VLDO28 Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_VLDO28_VOSEL						RG_VLDO28_VOCAL			
Type							RW						RW			
Reset							0	1					0	0	0	0

Bit(s)	Name	Description
9:8	RG_VLDO28_VOSEL	**Selects output voltage** 2'b01: 2.8V 2'b11: 3.0V
3:0	RG_VLDO28_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C2C **VIBR_ANA_CON0** **VIBR Control Register 0** **0900**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VIBR_VOSEL								RG_VIBR_VOCAL			
Type					RW								RW			
Reset					1	0	0	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VIBR_VOSEL	**Selects output voltage** 4'b0000: 1.2V 4'b0001: 1.3V 4'b0010: 1.5V 4'b0100: 1.8V 4'b0101: 2.0V 4'b1001: 2.8V 4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VIBR_VOCAL	**Calibrates output voltage** 4'b0000: +00mV

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C30 **VSIM1_ANA_CON0** **VSIM1 Control Register 0** **0406**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM1_VOSEL								RG_VSIM1_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	1	1	0

Bit(s)	Name	Description
11:8	RG_VSIM1_VOSEL	**Selects output voltage** 4'b0011: 1.7V 4'b0100: 1.8V 4'b1000: 2.7V 4'b1011: 3.0V 4'b1100: 3.1V
3:0	RG_VSIM1_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C34 **VSIM2_ANA_CON0** **VSIM2 Control Register 0** **0406**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM2_VOSEL								RG_VSIM2_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	1	1	0

Bit(s)	Name	Description
11:8	RG_VSIM2_VOSEL	**Selects output voltage** 4'b0011: 1.7V 4'b0100: 1.8V 4'b1000: 2.7V 4'b1011: 3.0V

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'b1100: 3.1V
3:0	RG_VSIM2_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C38 VMCH_ANA_CON0 VMCH Control Register 0 0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VMCH_VOSEL							RG_VMCH_VOCAL			
Type						RW							RW			
Reset						0	1	1					0	0	0	0

Bit(s)	Name	Description
10:8	RG_VMCH_VOSEL	**Selects output voltage** 3'b010: 2.9V 3'b011: 3.0V 3'b101: 3.3V
3:0	RG_VMCH_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C3C VMC_ANA_CON0 VMC Control Register 0 0B00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMC_VOSEL								RG_VMC_VOCAL			
Type					RW								RW			
Reset					1	0	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VMC_VOSEL	**Selects output voltage** 4'b0100: 1.8V 4'b1010: 2.9V

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VMC_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C40 **VCAMIO_ANA_CON0** **VCAMIO Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VCAMIO_VOCAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VCAMIO_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C44 **VCN18_ANA_CON0** **VCN18 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VCN18_VOCAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VCN18_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C48 **VRF18_ANA_CON0** **VRF18 Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VRF18_VOCAL			
Type													RW			
Reset													0	0	0	1

Bit(s)	Name	Description
3:0	RG_VRF18_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C52 **VRF12_ANA_CON0** **VRF12 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VRF12_VOCAL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_VRF12_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1C8C	VCAMA_ANA_CON0	VCAMA Control Register 0	0A00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMA_VOSEL								RG_VCAMA_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMA_VOSEL	**Selects output voltage** 4'b0111: 2.5V 4'b1010: 2.8V
3:0	RG_VCAMA_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C90	VEFUSE_ANA_CON0	VEFUSE Control Register 0	0400

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VEFUSE_VOSEL								RG_VEFUSE_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VEFUSE_VOSEL	**Selects output voltage** 4'b0000: 1.2V 4'b0001: 1.3V 4'b0010: 1.5V 4'b0100: 1.8V 4'b1001: 2.8V 4'b1010: 2.9V 4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VEFUSE_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1C94	VCAMD_ANA_CON0	VCAMD Control Register 0	0600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMD_VOSEL								RG_VCAMD_VOCAL			
Type					RW								RW			
Reset					0	1	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMD_VOSEL	**Selects output voltage** 4'b0100: 1.0V 4'b0101: 1.1V 4'b0110: 1.2V 4'b0111: 1.3V 4'b1001: 1.5V 4'b1100: 1.8V
3:0	RG_VCAMD_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1E10	XPP_TOP_CKPDN_CON0	XPP_TOP_CKPDN Control Register 0	001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_DRV_CHRIND_CK_PDN	RG_DRV_128K_CK_PDN			RG_DRV_ISINK1_CK_PDN	
Type											RW	RW			RW	
Reset											0	1			1	

Bit(s)	Name	Description
5	RG_DRV_CHRIND_CK_PDN	**Powers down DRV_CHRIND_CK** 0: Power on 1: Power down
4	RG_DRV_128K_CK_PDN	**Powers down DRV_128K_CK** 0: Power on 1: Power down
1	RG_DRV_ISINK1_CK_PDN	**Powers down DRV_ISINK1_CK** 0: Power on 1: Power down

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1E12	XPP_TOP_CKPDN_CON0_SET	XPP_TOP_CKPDN_CON0 Register SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKPDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKPDN_CON0_SET	**Sets up XPP_TOP_CKPDN_CON0** 1'b0: Not set 1'b1: Set

1E14	XPP_TOP_CKPDN_CON0_CLR	XPP_TOP_CKPDN_CON0 Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKPDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKPDN_CON0_CLR	**Clears XPP_TOP_CKPDN_CON0** 1'b0: Not clear 1'b1: Clear

1E16	XPP_TOP_CKSEL_CON0	XPP_TOP_CKSEL Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DRV_ISINK_CK_CKSEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DRV_ISINK_CK_CKSEL	**DRV_ISINK_CK clock selection** 1'b0: PMU128M_CK 1'b1: PMU32M_CK

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1E18	XPP_TOP_CKSEL_CON0_SET	XPP_TOP_CKSEL_CON0 Register SET	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKSEL_CON0_SET	**Sets up XPP_TOP_CKSEL_CON0** 1'b0: Not set 1'b1: Set

1E1A	XPP_TOP_CKSEL_CON0_CLR	XPP_TOP_CKSEL_CON0 Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XPP_TOP_CKSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XPP_TOP_CKSEL_CON0_CLR	**Clears XPP_TOP_CKSEL_CON0** 1'b0: Not clear 1'b1: Clear

1E88	ISINK1_CON0	ISINK1 Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM1_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM1_FSEL	**ISINK1 dimming frequency selection** freq: 128KHz 0: 500 Hz 1: 250 Hz 2: 167 Hz 3: 125 Hz 4: 100 Hz 5: 83 Hz 65535: 0.0076 Hz

1E8A	ISINK1_CON1	ISINK1 Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Name	ISINK_CH1_STEP			ISINK_DIM1_DUTY												
Type	RW			RW												
Reset	0	0	0	0	0	0	0	0	0	0	0					

Bit(s)	Name	Description
15:13	ISINK_CH1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
12:5	ISINK_DIM1_DUTY	**ISINK ON-duty of dimming 1 control** N: (N+1)/256 0: 1/256 1: 2/256 2: 3/256 255: 256/256

1E8C **ISINK1_CON2** ISINK1 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH1_TR1_SEL				ISINK_BREATH1_TR2_SEL				ISINK_BREATH1_TF1_SEL				ISINK_BREATH1_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH1_TR1_SEL	**Selects ISINK1 breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH1_TR2_SEL	**Selects ISINK1 breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH1_TF1_SEL	**ISINK1 breath mode falling time selection for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TF2_SEL	**ISINK1 breath mode falling time selection for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

1E8E **ISINK1_CON3** **ISINK1 Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH1_TON_SEL								ISINK_BREATH1_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH1_TON_SEL	**Selects ISINK1 breath mode Ton time** 0: 0.123s 1: 0.338s

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TOFF_SEL	**Selects ISINK1 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

1E94 **ISINK_SFSTR** **ISINK Soft Start** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ISINK_SFSTR1_TC		ISINK_SFSTR1_EN								
Type						RW		RW								
Reset						0	0	0								

Bit(s)	Name	Description
10:9	ISINK_SFSTR1_TC	**ISINK1 soft start timing step control** Freq: 128kHz 2'b00: 1T (7.8125us) 2'b01: 2T (15.625us) 2'b10: 3T (23.4375us) 2'b11: 4T (31.25us)
8	ISINK_SFSTR1_EN	**ISINK1 soft start control** 1'b0: Disable 1'b1: Enable soft start current step

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1E96 **ISINK_EN_CTRL** **ISINK Enable Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_CH1_BIAS_EN						ISINK_CHOP1_EN				ISINK_CH1_EN	
Type					RW						RW				RW	
Reset					0						0				0	

Bit(s)	Name	Description
11	ISINK_CH1_BIAS_EN	**Enables ISINK Channel 1 bias CLK** 1'b0: Disable 1'b1: Enable
5	ISINK_CHOP1_EN	**Enables ISINK Channel 1 CHOP CLK** 1'b0: Disable 1'b1: Enable
1	ISINK_CH1_EN	**Turns on ISINK Channel 1** 1'b0: Disable 1'b1: Enable

1E98 **ISINK_MODE_CTRL** **ISINK Mode Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ISINK_CH1_MODE								ISINK_CH1_PWM_MODE					
Type			RW								RW					
Reset			0	0							0					

Bit(s)	Name	Description
13:12	ISINK_CH1_MODE	**Selects ISINK Channel 1 enable mode** 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode
5	ISINK_CH1_PWM_MODE	**PWM on/off first control** 1'b0: PWM off-first mode 1'b1: PWM on-first mode

1E9A **DRIVER_ANA_CON0** **DRIVER Control Register 0** **CE00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_ISINK1_CHO									

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

							P_EN									
Type							RW									
Reset							1									

Bit(s)	Name	Description
9	RG_ISINK1_CHOP_EN	**Enables ISINK1 chopper** 0: Disable 1: Enable (default)

1E9C ISINK_ANA_CON0 ISINK Read-Only Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_ISINK1_STEP			DA_ISINK1_CHOP_CLK	DA_ISINK1_BIAS_EN	DA_ISINK1_EN
Type											RO			RO	RO	RO
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:3	DA_ISINK1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
2	DA_ISINK1_CHOP_CLK	
1	DA_ISINK1_BIAS_EN	
0	DA_ISINK1_EN	

1F08 CHRIND_CON0 CHRIND Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_DIM_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CHRIND_DIM_FSEL	**Selects ISINK0 dimming frequency** Freq: 128kHz 0: 500Hz 1: 250Hz 2: 167Hz 3: 125Hz

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		5: 83Hz

1F0A CHRIND_CON1 CHRIND Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CHRIND_DIM_DUTY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	CHRIND_DIM_DUTY	**ISINK ON-duty of dimmingo control** N: (N+1)/32 0: 1/256 1: 2/256 2: 3/256 255: 256/256

1F0C CHRIND_CON2 CHRIND Control Register 2 3000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_PWM_MODE	CHRIND_STEP														
Type	RW	RW														
Reset	0	0	1	1												

Bit(s)	Name	Description
15	CHRIND_PWM_MODE	1'b0: PWM off-first mode 1'b1: PWM on-first mode
14:12	CHRIND_STEP	**Coarse 6 step current level for chrind** 000: 2mA 001: 4mA 010: 4mA 011: 6mA 100: NA 101: NA 110: NA 111: NA

1F0E CHRIND_CON3 CHRIND Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_BREATH_TR1_SEL				CHRIND_BREATH_TR2_SEL				CHRIND_BREATH_TF1_SEL				CHRIND_BREATH_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:12	CHRIND_BREATH_TR1_SEL	**Selects CHRIND breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	CHRIND_BREATH_TR2_SEL	**Selects CHRIND breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	CHRIND_BREATH_TF1_SEL	**Selects CHRIND breath mode falling time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	CHRIND_BREATH_TF2_SEL	**Selects ISINK0 breath mode falling time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

1F10 **CHRIND_CON4** **CHRIND Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CHRIND_BREATH_TON_SEL								CHRIND_BREATH_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	CHRIND_BREATH_TON_SEL	**Selects CHRIND breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	CHRIND_BREATH_TOFF_SEL	**Selects CHRIND breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

1F12 **CHRIND_EN_CTRL** **CHRIND Enable Control Simple** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHRIND_MODE_SEL**						**CHRIND_BIAS_EN**		**CHRIND_MODE**		**CHRIND_CHOP_EN**	**CHRIND_EN**	**CHRIND_EN_SEL**	**CHRIND_SFSTR_TC**		**CHRIND_SFSTR_EN**
Type	RW						RW		RW		RW	RW	RW	RW		RW
Reset	0						0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	CHRIND_MODE_SEL	
9	CHRIND_BIAS_EN	**Enables ISINK Channel 2 bias CLK** 1'b0: Disable 1'b1: Enable
7:6	CHRIND_MODE	**Selects ISINK Channel 1 enable mode** 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode
5	CHRIND_CHOP_EN	**Enables ISINK Channel 3 CHOP CLK** 1'b0: Disable 1'b1: Enable
4	CHRIND_EN	**Turns on ISINK Channel 2** 1'b0: Disable 1'b1: Enable
3	CHRIND_EN_SEL	1'b0: Auto 1'b1: SW
2:1	CHRIND_SFSTR_TC	**ISINK3 soft start timing step control** Freq: 128kHz 2'b00: 1T (7.8125us) 2'b01: 2T (15.625us) 2'b10: 3T (23.4375us) 2'b11: 4T (31.25us)
0	CHRIND_SFSTR_EN	**ISINK3 soft start control** 1'b0: Disable 1'b1: Enable soft start current step

208C **AUD_TOP_CKPDN_CON0** **AUDIO CLK Power Down Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**RG_AUDNCP_CK_PDN**	**RG_ZCD13M_CK_PDN**			**RG_AUDIF_CK_PDN**	**RG_AUD_CK_PDN**	**RG_ACCDET_CK_PDN**
Type										RW	RW			RW	RW	RW
Reset										0	0			0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
6	RG_AUDNCP_CK_PDN	**Powers down AUDNCP_CK** 0: Power on 1: Power down
5	RG_ZCD13M_CK_PDN	**Powers down ZCD13M_CK** 0: Power on 1: Power down
2	RG_AUDIF_CK_PDN	**Powers down AUDIF_CK** 0: Power on 1: Power down
1	RG_AUD_CK_PDN	**Powers down AUD_CK** 0: Power on 1: Power down
0	RG_ACCDET_CK_PDN	**Powers down ACCDET_CK** 0: Power on 1: Power down

2092 **AUD_TOP_CKSEL_CON0** **AUDIO CKSEL Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_AUDIF_CK_CKSEL	RG_AUD_CK_CKSEL		
Type													RW	RW		
Reset													0	0		

Bit(s)	Name	Description
3	RG_AUDIF_CK_CKSEL	**Selects AUDIF_CK clock** 1'b0: R_AUD_CLK_MOSI 1'b1: R_AUD26M_CK
2	RG_AUD_CK_CKSEL	**Selects AUD_CK clock** 1'b0: R_AUD26M_CK 1'b1: R_AUD_CLK_MOSI

20B4 **AUDNCP_CLKDIV_CON0** **AUDNCP_CLKDIV Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_CHG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_CHG	**Divider change enable signal**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		Toggle this bit will change ncp div value to ncp counters.

20B6 **AUDNCP_CLKDIV_CON1** **AUDNCP_CLKDIV Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_ON
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_ON	**Divider enable bit** Set it to 1'b1 to enable ncp.

20B8 **AUDNCP_CLKDIV_CON2** **AUDNCP_CLKDIV Control Register 2** **002C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_DIVCKS_PRG								
Type								RW								
Reset								0	0	0	1	0	1	1	0	0

Bit(s)	Name	Description
8:0	RG_DIVCKS_PRG	ncp divider program register

20BA **AUDNCP_CLKDIV_CON3** **AUDNCP_CLKDIV Control Register 3** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_PWD_NCP
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_DIVCKS_PWD_NCP	power do

20BC **AUDNCP_CLKDIV_CON4** **AUDNCP_CLKDIV Control Register 4** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Name															**RG_DIVCKS_PWD_NCP_ST_SEL**	
Type															RW	
Reset															1	0

Bit(s)	Name	Description
1:0	RG_DIVCKS_PWD_NCP_ST_SEL	**Selects ncp soft start time** 2'b00: 50us 2'b01: 100us 2'b10: 150us 2'b11: 200us

20BE **AUD_TOP_MON_CON0** **AUD_TOP_MON Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_AUD_CLK_INT_MON_FLAG_EN**	**RG_AUD_CLK_INT_MON_FLAG_SEL**										
Type					RW	RW										
Reset					0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
11	RG_AUD_CLK_INT_MON_FLAG_EN	Enables accdet monitor flag
10:3	RG_AUD_CLK_INT_MON_FLAG_SEL	Selects accdet monitor flag

2108 **AFE_UL_DL_CON0** **Audio UL and DL Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**afe_ul_lr_swap**	**afe_dl_lr_swap**														**afe_on**
Type	RW	RW														RW
Reset	0	0														0

Bit(s)	Name	Description
15	afe_ul_lr_swap	Swaps audio UL L/R channel before UL SRC
14	afe_dl_lr_swap	Swaps audio DL L/R channel before DAC FIFO
0	afe_on	Audio UL and DL turn on

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

210A **AFE_DL_SRC2_CON0_L** **AFE_DL_SRC2 Control Register 0 Low Part** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																dl_2_src_on_tmp_ctl_pre
Type																RW
Reset																0

Bit(s)	Name	Description
0	dl_2_src_on_tmp_ctl_pre	Turns on down-link

210C **AFE_UL_SRC_CON0_H** **AFE uplink SRC Control Register 0 High Part** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			c_digmic_phase_sel_ch1_ctl			c_digmic_phase_sel_ch2_ctl			c_two_digital_mic_ctl							
Type			RW			RW			RW							
Reset			0	0	0	0	0	0	0							

Bit(s)	Name	Description
13:11	c_digmic_phase_sel_ch1_ctl	**Selects 8 input phase latch**
10:8	c_digmic_phase_sel_ch2_ctl	**Selects 8 input phase latch**
7	c_two_digital_mic_ctl	**Turns on dual digital microphones mode** 0: Turn off 1: Turn on

210E **AFE_UL_SRC_CON0_L** **AFE uplink SRC Control Register 0 Low Part** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmic_low_power_mode_ctl										digmic_3p25m_1p625m_sel_ctl			ul_loop_back_mode_ctl	ul_sdm_3_level_ctl	ul_src_on_tmp_ctl
Type	RW										RW			RW	RW	RW
Reset	0	0									0			0	0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:14	dmic_low_power_mode_ctl	**Digital mic low power mode** 0: Original mode 1: 1.625m 48k mode 2: 812.5k low power mode 3: 406.25k low power mode
5	digmic_3p25m_1p625m_sel_ctl	**Digmic input mode 1** 0: 3.25M mode 1: 1.625M mode
2	ul_loop_back_mode_ctl	**Enables loopback mode from DL** 0: Normal UL 1: Loopback from DL
1	ul_sdm_3_level_ctl	**Selects SDM 3-level mode (digital MIC data path), first priority choice** 0: De-select SDM 3-level mode 1: Select SDM 3-level mode
0	ul_src_on_tmp_ctl	**Turns on uplink SRC** 0: Turn off 1: Turn on

2110 **AFE_TOP_CON0** **AFE Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ul_sine_on	dl_sine_on
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	ul_sine_on	**Enables ul sine table** 0: UL from up8x_rxif normal path 1: UL from sinetable
0	dl_sine_on	**Enables dl sine table** 0: DL from up8x_rxif normal path 1: DL from sinetable

2112 **AUDIO_TOP_CON0** **AUDIO Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pdn_afe_ctl	pdn_dac_ctl	pdn_adc_ctl		pdn_i2s_dl_ctl	pwr_clk_dis_ctl	pdn_afe_testmodel_ctl	pdn_reserved
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
7	pdn_afe_ctl	**Powers down afe** 0: Not power down 1: Power down
6	pdn_dac_ctl	**Powers down down-link** 0: Not power down 1: Power down
5	pdn_adc_ctl	**Powers down up-link** 0: Not power down 1: Power down
3	pdn_i2s_dl_ctl	**Reserved**
2	pwr_clk_dis_ctl	**Disables total audio clk** 0: Not power down 1: Power down
1	pdn_afe_testmodel_ctl	**Powers down some built-in testing model clock source** 0: Not power down 1: Power down
0	pdn_reserved	0: Not power down 1: Power down

2114 AFE_MON_DEBUG0 AFE Monitor Output Debug Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_sys_top_mon_swap			audio_sys_top_mon_sel									afe_mon_sel			
Type	RW			RW									RW			
Reset	0	0		0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15:14	audio_sys_top_mon_swap	**Swaps monitor output from 32 bits to 8 bits** 0: mon_out[7:0] 1: mon_out[15:8] 2: mon_out[23:16] 3: mon_out[31:24]
12:8	audio_sys_top_mon_sel	**Selects monitor output of audio system top level**
3:0	afe_mon_sel	**Selects monitor output of afe level**

2116 AFUNC_AUD_CON0 A_FUNC AUDIO Control Register 0 D821

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cci_aud_anack_sel	cci_audio_fifo_wptr			cci_scrambler_cg_en	cci_lch_inv	cci_rand_en	cci_spltscrmb_clk_on	cci_spltscrmb_on	cci_aud_idac_test_en	cci_zero_pad_disable	cci_aud_split_test_en	cci_aud_sdm_mutel	cci_aud_sdm_muter	cci_aud_sdm_7bit_sel	cci_scrambler_en
Type	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	0	1	1	0	0	0	0	0	1	0	0	0	0	1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15	cci_aud_anack_sel	**Analog 13m source inversion option** 0: Not invert AD_AUDDEC_13M_D5N_VCORE (or GPI) 1: Invert
14:12	cci_audio_fifo_wptr	**audio_fifo write pointer initial value**
11	cci_scrambler_cg_en	**Enables scrambler PA** 0: Disables scrambler PA 1: Enables scrambler PA
10	cci_lch_inv	**Selects sdm left channel out of phase** 0: In-phase with right channel 1: Out-of-phase with right channel
9	cci_rand_en	**Enables scrambler random** 0: Not random 1: Random
8	cci_splt_scrmb_clk_on	**Scrambler clock on** 0: Off 1: On
7	cci_splt_scrmb_on	**Enables scrambler output** 0: Off 1: On
6	cci_aud_idac_test_en	**Enables scrambler output test** 0: Normal path 1: From test_in
5	cci_zero_pad_disable	**Disables scrambler zero padding** 0: Zero-padding 1: Disable zero-padding
4	cci_aud_split_test_en	**Enables splitter test** 0: Normal path 1: From test_in ([12:8]/[7:4]/[2:0])
3	cci_aud_sdm_mutel	**Enables sdm output mute for left channel, control by AFUNC_AUD_CON1[15:8]** 0: Not control by AFUNC_AUD_CON1 1: Control by AFUNC_AUD_CON1
2	cci_aud_sdm_muter	**Enables sdm output mute for left channel, control by AFUNC_AUD_CON1[7:0]** 0: Not control by AFUNC_AUD_CON1 1: Control by AFUNC_AUD_CON1
1	cci_aud_sdm_7bit_sel	**Selects splitter** 0: From splitter 1 1: From splitter 3
0	cci_scrambler_en	**Enables scrambler** 0: Disable 1: Enable

2118 **AFUNC_AUD_CON1** **A_FUNC AUDIO Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aud_sdm_test_l								aud_sdm_test_r							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:8	aud_sdm_test_l	sdm mute test value for left channel
7:0	aud_sdm_test_r	sdm mute test value for right channel

211A **AFUNC_AUD_CON2** **A_FUNC AUDIO Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									cci_aud_dac_ana_mute	cci_aud_dac_ana_rstb_sel		cci_audio_fifo_clkin_inv	cci_audio_fifo_enable	cci_acd_mode	cci_afifo_clk_pwdb	cci_acd_func_rstb
Type									RW	RW		RW	RW	RW	RW	RW
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	cci_aud_dac_ana_mute	**Analog DAC interface mute (RG) control** 0: Analog DAC interface input from aud_dac_ana output (normal) 1: Analog DAC interface input from fixed mute patterns
6	cci_aud_dac_ana_rstb_sel	**Enables aud_dac_ana soft_rstb source selection** 0: aud_dac_ana reset by global rstb 1: aud_dac_ana reset by global rstb and cci_acd_func_rstb
4	cci_audio_fifo_clkin_inv	**Selects sdm 6.5M clock phase** 0: In-phase 1: Out-of-phase
3	cci_audio_fifo_enable	**Enables sdm audio_fifo** 0: Disable 1: Enable
2	cci_acd_mode	**sdm audio_fifo analog FT test mode** 0: Normal path 1: Test path from GPI, clock and data will be from GPI, for selection see sdm_testck_src_sel.
1	cci_afifo_clk_pwdb	**sdm audio_fifo clock power down bit** 0: Power down 1: Power on
0	cci_acd_func_rstb	**sdm audio_fifo rstb bit** 0: Reset 1: Released

211C **AFUNC_AUD_CON3** **A_FUNC AUDIO Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdm_ana13M_testck_sel	sdm_ana13M_testck_src_sel				sdm_testck_src_sel				digmic_testck_src_sel						digmic_testck_sel
Type	RW	RW				RW				RW						RW
Reset	0	0	0	0		0	0	0		0	0	0				0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15	sdm_ana13M_testck_sel	**Selects sdm testck from GPI** 0: Normal path from digital output 1: Testing path from GPI. See the descriptions of sdm_ana13M_testck_src_sel for details.
14:12	sdm_ana13M_testck_src_sel	**Selects different GPI as sdm testck source** 0: test_ck_i[3] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[0] 5: test_in_i[1] 6: test_in_i[3] 7: test_in_i[5]
10:8	sdm_testck_src_sel	**Selects different GPI as sdm testck source** 0: test_ck_i[3] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[0] 5: test_in_i[1] 6: test_in_i[3] 7: test_in_i[5]
6:4	digmic_testck_src_sel	**Selects different GPI as digmic testck source** 0: test_ck_i[3] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[2] 5: test_in_i[4] 6: test_in_i[6] 7: test_in_i[7]
0	digmic_testck_sel	**Selects digmic testck from GPI** 0: Normal path from digital output 1: Testing path from GPI. See the descriptions of digmic_testck_src_sel for details.

211E **AFUNC_AUD_CON4** **A_FUNC AUDIO Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ul_fifo_wclk_inv		ul_fifo_digmic_wdata_testsrc_sel	ul_fifo_wdata_testen	ul_fifo_wdata_testsrc_sel	ul_fifo_wclk_6p5m_testck_sel	ul_fifo_wclk_6p5m_testck_src_sel		
Type								RW		RW	RW	RW	RW	RW		
Reset								0		0	0	0	0	0	0	0

Bit(s)	Name	Description
8	ul_fifo_wclk_inv	**Selects inverse ul FIFO wclk** 0: Not invert 1: Invert ul FIFO wclk

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
6	ul_fifo_digmic_wdata_testsrc_sel	**Selects ul FIFo digmic wdata from GPI (Test_in[1:0]) or tri-gen:** ch1: Test_in[1] ch2: Test_in[0] 0: Testing path from test input GPI, i.e. left channel ch1= test_in[1], right channel ch2 = test_in[0]. 1: Testing path from built-in tri-gen, ch1 uses tri_out[1], ch2 uses tri_out[0].
5	ul_fifo_wdata_testen	**Selects ul FIFO wdata from others** 0: Normal path from analog output 1: Testing path from test input. See the descriptions of ul_fifo_wdata_testsrc_sel for details.
4	ul_fifo_wdata_testsrc_sel	**Enables GPI as ul FIFO write testck source** 0: Test input from GPI, i.e., Left channel ch1[4:0]= test_in[4:0], right channel ch2[4:0] = test_in[4:0]. 1: Test input from tri-gen, both ch1 and ch2 using the same inputs from tri-gen
3	ul_fifo_wclk_6p5m_testck_sel	**Enable GPI as ul fifo write testck source** 0: Normal path from analog 6p5M 1: From testck described in ul_fifo_wclk_6p5m_testck_src_sel
2:0	ul_fifo_wclk_6p5m_testck_src_sel	**Selects different GPI as ul FIFO write testck source** 0: test_ck_i[2] 1: test_ck_i[2] 2: test_ck_i[1] 3: test_ck_i[0] 4: test_in_i[5] 5: test_in_i[6] 6: test_in_i[7] 7: test_in_i[0]

2120 **AFUNC_AUD_CON5** **A_FUNC AUDIO Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r_aud_dac_pos_large_mono								r_aud_dac_neg_large_mono							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	r_aud_dac_pos_large_mono	pos_lareg to DAC
7:0	r_aud_dac_neg_large_mono	neg_lareg to DAC

2122 **AFUNC_AUD_CON6** **A_FUNC AUDIO Control Register 6** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r_aud_dac_pos_small_mono				r_aud_dac_neg_small_mono				r_aud_dac_pos_tiny_mono		r_aud_dac_neg_tiny_mono		r_aud_dac_mono_sel			r_aud_dac_swrstb
Type	RW				RW				RW		RW		RW			RW

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			1

Bit(s)	Name	Description
15:12	r_aud_dac_pos_small_mono	**pos_small to DAC**
11:8	r_aud_dac_neg_small_mono	**neg_small to DAC**
7:6	r_aud_dac_pos_tiny_mono	**pos_tiny to DAC**
5:4	r_aud_dac_neg_tiny_mono	**neg_tiny to DAC**
3	r_aud_dac_mono_sel	**Uses mono register value to test DAC** 0: Not use mono register value 1: Use mono register value
0	r_aud_dac_sw_rstb	**SDM sync soft reset** 0: reset SDM 1: no reset SDM

2124 AFUNC_AUD_MON0 A_FUNC AUDIO Monitor Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aud_scr_out_l								aud_scr_out_r							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	aud_scr_out_l	Scrambler/splitter debug output to read bus
7:0	aud_scr_out_r	Scrambler/splitter debug output to read bus

2126 AUDRC_TUNE_MON0 Analog Monitor Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	async_test_out_bck			RGS_AUDRCTUNE1READ								RGS_AUDRCTUNE0READ				
Type	RU			RU								RU				
Reset	0			0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15	async_test_out_bck	
12:8	RGS_AUDRCTUNE1READ	AUDIOEN RC TUNE OUTPUT TO READ for 1 channel
4:0	RGS_AUDRCTUNE0READ	AUDIOEN RC TUNE OUTPUT TO READ for 0 channel

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2140 **AFE_SGEN_CFG0** **AFE SGEN CON0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_amp_div_ch1_ctl								c_dac_en_ctl	c_mute_sw_ctl						
Type	RW								RW	RW						
Reset	0	0	0	0					0	0						

Bit(s)	Name	Description
15:12	c_amp_div_ch1_ctl	**Amplitude setting of channel 1 (SGEN)** 0: 0dB full scale 1: -6dB 2: -12dB 3: -18dB 4: -24dB 5: -30dB 6: -36dB 7: -42dB 8: -48dB 9: -54dB 10: -60dB 11: -66dB 12: -72dB 13: -78dB 14: -84dB 15: -90dB
7	c_dac_en_ctl	**Makes voice DAC output the test sine wave, signal generator (SGEN) configure** 0: Disable sine waves output 1: Voice DAC inputs are sine waves
6	c_mute_sw_ctl	**Mute switch (SGEN)** 0: Turn on the sine wave output in this test mode 1: Mute the sine wave output

2142 **AFE_SGEN_CFG1** **AFE SGEN CON1** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	c_sgen_rch_inv_5bit	c_sgen_rch_inv_8bit										c_freq_div_ch1_ctl				
Type	RW	RW										RW				
Reset	0	0										0	0	0	0	1

Bit(s)	Name	Description
15	c_sgen_rch_inv_5bit	**Inverts RCH sgen 5-bit data output**
14	c_sgen_rch_inv_8bit	**Inverts RCH sgen 8-bit data output**
4:0	c_freq_div_ch1_ctl	**Frequency setting of channel 1, 1X~15X for voice, 1X~31X for audio** **Frequency = Sampling rate/64*FREQ_DIV (SGEN)**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		Sample rate: UL (8K/16K/32K -> 64K; 48K -> 96K); DL (8xFS)

2144 **AFE_ADC_ASYNC_FIFO_CFG** **AFE_ADC_SYNC_FIFO_CFG** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**rg_ul_async_fifo_soft_rst_en**	**rg_ul_async_fifo_soft_rst**			**rg_amic_ul_adc_clk_sel**	
Type											RW	RW			RW	
Reset											0	1			0	

Bit(s)	Name	Description
5	rg_ul_async_fifo_soft_rst_en	**Selects UL async FIFO soft reset** 0: UL async FIFO uses global reset. 1: UL async FIFO uses soft reset.
4	rg_ul_async_fifo_soft_rst	**UL soft reset control** 0: UL FIFO soft reset 1: Normal
1	rg_amic_ul_adc_clk_sel	**Selects ADC 0/1 channel latch clk** 0: ana_ch0 ck selected 1: ana_ch1 ck selected

2146 **AFE_DCCLK_CFG0** **AFE_DCCLK_CFG0** **0FE2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**dcclk_div**											**dcclk_inv**			**dcclk_pdn**	**dcclk_gen_on**
Type	RW											RW			RW	RW
Reset	0	0	0	0	1	1	1	1	1	1	1	0			1	0

Bit(s)	Name	Description
15:5	dcclk_div	**dcclk divider:** dcclk = 13M(12.854M)/(div+1)
4	dcclk_inv	**dcclk inverter**
1	dcclk_pdn	**dcclk power down control** 0: dcclk output 1: dcclk power down
0	dcclk_gen_on	**Enables dcclk generation** 0: Disable 1: Enable

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2148 **AFE_DCCLK_CFG1** **AFE_DCCLK_CFG1** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					resync_src_sel		resync_src_ck_inv	dcclk_resync_bypass	dcclk_phase_sel							
Type					RW		RW	RW	RW							
Reset					0	0	0	1	0	0	0	0				

Bit(s)	Name	Description
11:10	resync_src_sel	**Selects dcclk resync clock** 00: adcsync_clk 01: vow 12.854M 10: buck_oscclk 11: 26m clock
9	resync_src_ck_inv	**dcclk resync clock inverter**
8	dcclk_resync_bypass	**dcclk bypass resync** 0: Resync 1: Bypass resync
7:4	dcclk_phase_sel	**Selects dcclk resync phase**

2188 **AUDENC_ANA_CON0** **AUDENC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCLINPUTSEL		RG_AUDADCLPWRUP		RG_AUDPREAMPLGAIN			RG_AUDPREAMPLINPUTSEL		RG_AUDPREAMPLVSCALE		RG_AUDPREAMPLPGATEST	RG_AUDPREAMPLDCRPECHARGE	RG_AUDPREAMPLDCCEN	RG_AUDPREAMPLON
Type		RW		RW		RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCLINPUTSEL	**Selects audio L ADC input** 00: Idle 01: AIN0 10: Left preamplifier 11: Idle
12	RG_AUDADCLPWRUP	**Powers up audio L ADC** 0: Power down 1: Power on
10:8	RG_AUDPREAMPLGAIN	**Adjusts audio L preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
7:6	RG_AUDPREAMPLINPUTSEL	**Selects audio L preamplifier input** 00: None

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPL VSCALE	**Audio L preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPL PGATEST	**Enables audio L preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPL DCRPECHARGE	**Audio L preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPL DCCEN	**Audio L DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPL ON	**Enables audio L preamplifier** 0: Disable 1: Enable

218A **AUDENC_ANA_CON1** **AUDENC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCRINPUTSEL		RG_AUDADCRPWRUP		RG_AUDPREAMPRGAIN			RG_AUDPREAMPRINPUTSEL		RG_AUDPREAMPRVSCALE		RG_AUDPREAMPRPGATEST	RG_AUDPREAMPRDCRPECHARGE	RG_AUDPREAMPRDCCEN	RG_AUDPREAMPRON
Type		RW		RW		RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCRINPUTSEL	**Selects audio R ADC input** 00: Idle 01: AIN0 10: Right preamplifier 11: Idle
12	RG_AUDADCRPWRUP	**Powers up audio R ADC** 0: Power down 1: Power on
10:8	RG_AUDPREAMPRGAIN	**Adjusts audio R preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
7:6	RG_AUDPREAMPRINPUTSEL	**Selects audio R preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPR	**Audio R preamplifier PGA DC output voltage scale**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	VSCALE	
3	RG_AUDPREAMPRPGATEST	**Enables audio R preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPRDCRPECHARGE	**Audio R preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPRDCCEN	**Audio R DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPRON	**Enables audio R preamplifier** 0: Disable 1: Enable

218C **AUDENC_ANA_CON2** **AUDENC Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCFLASHIDDTEST		RG_AUDADCREFBUFIDDTEST		RG_AUDADC2NDSTAGEIDDTEST		RG_AUDADC1STSTAGEIDDTEST		RG_AUDPREAMPIDDTEST							
Type	RW		RW		RW		RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0						

Bit(s)	Name	Description
15:14	RG_AUDADCFLASHIDDTEST	**Selects audio ADC flash Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
13:12	RG_AUDADCREFBUFIDDTEST	**Selects audio ADC reference buffer Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
11:10	RG_AUDADC2NDSTAGEIDDTEST	**Audio ADC 2nd and 3rd Stage Idd adjustment bits** 00: 100% 01: 80% 10: 120% 11: 140%
9:8	RG_AUDADC1STSTAGEIDDTEST	**Audio ADC 1st Stage Idd adjustment bits** 00: 100% 01: 80% 10: 120% 11: 140%
7:6	RG_AUDPREAMPIDDTEST	**Audio preamplifier Idd adjustment bits** 00: 100% 01: 75% 10: 125% 11: 150%

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

218E **AUDENC_ANA_CON3** **AUDENC Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_PGABODYSW	RG_CMSTBENH			RG_AUDPREAMPAAFEN					RG_AUDADCCLKSOURCE		RG_AUDADCCLKSEL	RG_AUDADCDAC0P25FS
Type				RW	RW			RW					RW		RW	RW
Reset				0	0			0					0	0	0	0

Bit(s)	Name	Description
12	RG_PGABODYSW	**Audio PGA DCC mode body switch** 0: Body connected to GND (default) 1: Connect to VCM (DCCEN should be 1)
11	RG_CMSTBENH	**PGA common mode STB enhancement**
8	RG_AUDPREAMPAAFEN	**Audio preamplifier PGA with AAF input in DC couple mode** 0: Disable 1: Enable
3:2	RG_AUDADCCLKSOURCE	**Audio ADC clock source** 00: 26MHz from CLKSQ 01: 26MHz from CLKSQ test 10: 12.58MHz from 32kHz PLL 11: None
1	RG_AUDADCCLKSEL	**Selects audio ADC clock** 0: 6.5MHz clock in, 3.25MHz data out 1: 13MHz clock in, 6.5MHz data out
0	RG_AUDADCDAC0P25FS	**Enables audio ADC FBDAC 0.25FS** 0: 6.5MHz clock in, 3.25MHz data out 1: 3.25MHz clock in, 1.625MHz data out

2190 **AUDENC_ANA_CON4** **AUDENC Control Register 4** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDADCDACTEST	RG_AUDADCNODEM	RG_AUDADCDACNRZ	RG_AUDADCDACIDTEST		RG_AUDADCDACFBCURRENT	RG_AUDADCFFBYPASS	RG_AUDADCBYPASS	RG_AUDADCNOPATEST	RG_AUDADCWIDECM	RG_AUDADCFSRESET	RG_AUDADC3RDSTAGERESET	RG_AUDADC2NDSTAGERESET	RG_AUDADC1STSTAGESDENB
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	RG_AUDADCDACTEST	**Audio ADC DAC test** 0: Disable 1: Enable the data in RG_AUDADCTESTDATA[15:0] to be passed to DAC
12	RG_AUDADCNODEM	**Audio ADC DEM test**
11	RG_AUDADCDACN	**Audio ADC DAC in non return to zero mode**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	RZ	0: RZ mode (2I) 1: NRZ mod (I)
10:9	RG_AUDADCDACIDDTEST	**Selects audio ADC-DAC Idd current test** 00: Normal 11: -20% DAC f/b current
8	RG_AUDADCDACFBCURRENT	**Audio ADC feedback coefficient**
7	RG_AUDADCFFBYPASS	**Bypasses audio ADC feed forward** 0: Not bypass. Allow feedforward coefficient to pass signal to ADC flash 1: Bypass. Not allow ADC i/p signal to feedforward flash
6	RG_AUDADCBYPASS	**Enables audio ADC input resistor bypass** 0: Disable 1: Enable
5	RG_AUDADCNOPATEST	**Audio ADC no preamp test** 0: Normal ADC gain 1: 6dB ADC gain
4	RG_AUDADCWIDECM	**Enables audio ADC wide common mode** 0: Normal 1: Enable
3	RG_AUDADCFSRESET	**Selects audio encoder FS reset block model**
2	RG_AUDADC3RDSTAGERESET	**Audio ADC 3rd stage reset** 0: Normal 1: Reset
1	RG_AUDADC2NDSTAGERESET	**Audio ADC 2nd stage reset** 0: Normal 1: Reset
0	RG_AUDADC1STSTAGESDENB	**Audio ADC 1st stage source degenerate enableb** 0: Enable 1: Disable

2192 **AUDENC_ANA_CON5** **AUDENC Control Register 5** **1515**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDRCTUNERSEL	RG_AUDRCTUNER							RG_AUDRCTUNELSEL	RG_AUDRCTUNEL				
Type			RW	RW							RW	RW				
Reset			0	1	0	1	0	1			0	1	0	1	0	1

Bit(s)	Name	Description
13	RG_AUDRCTUNERSEL	**Selects audio R ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]
12:8	RG_AUDRCTUNER	**Audio R ADC RC tuned value** See RG_AUDRCTUNELSE.
5	RG_AUDRCTUNELSEL	**Selects audio L ADC RC tuning** 0: Use auto cal tune bits

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		1: Use RG_AUDRCTUNEL[4:0]
4:0	RG_AUDRCTUNEL	**Audio L ADC RC tuned value** See RG_AUDRCTUNELSE.

2194 **AUDENC_ANA_CON6** **AUDENC Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDENCSPARE						RG_AUDSPARE					RG_CM_REFGENSEL	RG_CLKSQ_IN_SEL_TEST	RG_CLKSQ_EN
Type			RW						RW					RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
13:8	RG_AUDENCSPARE	**RG_AUDENCSPARE[5:0]** [0] MON_SW_ON (ADA_NS_ACCDET2AUX_IN5; MICBIAS1_DCMONTOR) [1] MON_SW_ON (QS_AVDD18_ENC; MICBIAS1_DCMONTOR) [5:2] Spare control bits for encoder top
7:4	RG_AUDSPARE	**Spare control bits for PGA+ADC** [0] RG_RESETSEL: ADC reset selection [3:1] Spare control bits for encoder top
2	RG_CM_REFGENSEL	**Selects Audio uplink common voltage** 0: Default 1: Selection
1	RG_CLKSQ_IN_SEL_TEST	**Audio CLK source** CLKSQ IN SEL. (0): PAD_CLK26M, (1): NS_XO_AUDIO26M_CK 0: Use internal CLK(DCXO) 1: Use external CLK
0	RG_CLKSQ_EN	**Enables CLKSQ** 0: Off 1: On

2196 **AUDENC_ANA_CON7** **AUDENC Control Register 7** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVMIC				RG_DMICMONSEL			RG_DMICMONEN	RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_DMICHPCLKEN	RG_AUDDIGMICBIAS		RG_AUDDIGMICEN
Type	RW				RW			RW	RW		RW		RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_AUDSPAREVM	**Spare control bits for AVDD25MIC voltage domain**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	IC	
11:9	RG_DMICMONSEL	**Digital microphone monitor path**
8	RG_DMICMONEN	**Enables digital microphone monitor path** 0: Disable 1: Enable
7:6	RG_AUDDIGMICNDUTY	**Digital microphone negative duty control**
5:4	RG_AUDDIGMICPDUTY	**Digital microphone positive duty control**
3	RG_DMICHPCLKEN	**Digital microphone CLK source from** 0: Digital 1: CLKSQ
2:1	RG_AUDDIGMICBIAS	**Digital microphone slew rate control** 11 > 10 > 01 > 00
0	RG_AUDDIGMICEN	**Enables digital microphone** 0: Disable 1: Enable

2198 **AUDENC_ANA_CON8** **AUDENC Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDMICBIAS0DCSW2NEN	RG_AUDMICBIAS0DCSW2P2EN	RG_AUDMICBIAS0DCSW2P1EN		RG_AUDMICBIAS0DCSW0NEN	RG_AUDMICBIAS0DCSW0P2EN	RG_AUDMICBIAS0DCSW0P1EN		RG_AUDMICBIAS0VREF					RG_AUDMICBIAS0BYPASSEN	RG_AUDPWDBMICBIAS0
Type		RW	RW	RW		RW	RW	RW		RW					RW	RW
Reset		0	0	0		0	0	0		0	0	0			0	0

Bit(s)	Name	Description
14	RG_AUDMICBIAS0DCSW2NEN	**MIC Bias 0 DC couple switch 2N** 0: Off 1: On
13	RG_AUDMICBIAS0DCSW2P2EN	**MIC Bias 0 DC couple switch 2P2** 0: Off 1: On
12	RG_AUDMICBIAS0DCSW2P1EN	**MIC Bias 0 DC couple switch 2P1** 0: Off 1: On
10	RG_AUDMICBIAS0DCSW0NEN	**MIC Bias 0 DC couple switch 0N** 0: Off 1: On
9	RG_AUDMICBIAS0DCSW0P2EN	**MIC Bias 0 DC couple switch 0P2** 0: Off 1: On
8	RG_AUDMICBIAS0DCSW0P1EN	**MIC Bias 0 DC couple switch 0P1** 0: Off 1: On

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
6:4	RG_AUDMICBIAS0VREF	**Selects MIC Bias 0 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: Test 2.6V 111: Test 2.7V
1	RG_AUDMICBIAS0BYPASSEN	**Enables MIC Bias 0 BYPASS 2P8V** 0: Disable 1: Enable
0	RG_AUDPWDBMICBIAS0	**Powers down MIC Bias 0** 0: Power down 1: Power on

219A **AUDENC_ANA_CON9** **AUDENC Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MTEST_CURRENT	RG_MTEST_SEL	RG_MTEST_EN	RG_BANDGAPGEN			RG_AUDMICBIAS1DCSW1NEN	RG_AUDMICBIAS1DCSW1PEN		RG_AUDMICBIAS1VREF					RG_AUDMICBIAS1BYPASSEN	RG_AUDPWDBMICBIAS1
Type	RW	RW	RW	RW			RW	RW		RW					RW	RW
Reset	0	0	0	0			0	0		0	0	0			0	0

Bit(s)	Name	Description
15	RG_MTEST_CURRENT	**Moisture test mode using current mode** 0: Normal mode 1: Current sinks to PAD_HP_EINT
14	RG_MTEST_SEL	**Selects moisture test mode** 0: PAD_HP_EINT 1: PAD_ACCDET
13	RG_MTEST_EN	**Enables moisture test mode** 0: Normal mode 1: Moisture test current mode (ACCDET to AUXADC should be off)
12	RG_BANDGAPGEN	**Remote sense to bandgap ground** 0: Disable 1: Enable
9	RG_AUDMICBIAS1DCSW1NEN	**MIC Bias 1 DC couple switch 1N** 0: Off 1: On
8	RG_AUDMICBIAS1DCSW1PEN	**MIC Bias 1 DC couple switch 1P** 0: Off 1: On
6:4	RG_AUDMICBIAS1VREF	**Selects MIC Bias 1 Output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		100: 2.1V 101: 2.5V 110: Test 2.6V 111: Test 2.7V
1	RG_AUDMICBIAS1BYPASSEN	**Enables MIC Bias 1 BYPASS 2P8V** 0: Disable 1: Enable
0	RG_AUDPWDBMICBIAS1	**Powers down MIC Bias 1** 0: Power down 1: Power on

219C **AUDENC_ANA_CON10** **AUDENC Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ACCDET2AUXSWEN	RG_ACCDET2AUXBUFFERBYPASS	RG_ACCDET2AUXRESBYPASS	RG_EINTHIRENB	RG_EINTCONFIGACCDET	RG_EINTCOMPVTH	RG_SWBUFSWEN	RG_SWBUFMODSEL	RG_ACCDETSEL	RG_AUDACCDETTVDET	RG_AUDACCDETVTHBCAL	RG_AUDACCDETVTHACAL		RG_AUDACCDETVIN1PULLLOW	RG_AUDACCDETMICBIAS1PULLLOW	RG_AUDACCDETMICBIAS0PULLLOW
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15	RG_ACCDET2AUXSWEN	**Enables switch of ACCDET to AUXADC** 0: Off 1: On
14	RG_ACCDET2AUXBUFFERBYPASS	**Bypasses ACCDET to AUXADC buffer** 0: Normal 1: Bypass
13	RG_ACCDET2AUXRESBYPASS	**Bypasses ACCDET to AUXADC resistors** 0: Normal 1: Bypass
12	RG_EINTHIRENB	**Selects EINT High R** 0: 2M 1: 500k
11	RG_EINTCONFIGACCDET	**Internal connection between ACCDET and EINT** 0: Disable 1: Enable (EINT connect with ACCDET pin and ACCDETSEL should be 1)
10	RG_EINTCOMPVTH	**EINT comparator threshold** 0: 6/8 => 2.4V 1: 5/8 => 2V
9	RG_SWBUFSWEN	**Switch buffer turn on SW mode control for ACCDET to AUXADC** 0: Power down 1: Power on
8	RG_SWBUFMODSEL	**Buffer power control** 0: Hardware mode 1: Software mode
7	RG_ACCDETSEL	**Selects ACCDET input**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		0: ACCDET pin 1: MICP pin
6	RG_AUDACCDETTVDET	**Puts audio accessory detection into TV mode** 0: Disable 1: Enable
5	RG_AUDACCDETVTHBCAL	**Audio accessory detection voltage threshold B calibration**
4	RG_AUDACCDETVTHACAL	**Audio accessory detection voltage threshold A calibration**
2	RG_AUDACCDETVIN1PULLLOW	**Pulls low VIN1 pads when MICBIAS is off** 0: Disable 1: Enable
1	RG_AUDACCDETMICBIAS1PULLLOW	**Pulls low MIC Bias 1 pads when MICBIAS is off** 0: Disable 1: Enable
0	RG_AUDACCDETMICBIAS0PULLLOW	**Pulls low MIC Bias 0 pads when MICBIAS is off** 0: Disable 1: Enable

219E **AUDENC_ANA_CON11** **AUDENC Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_AUDRCTUNERREAD								RGS_AUDRCTUNELREAD				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
12:8	RGS_AUDRCTUNERREAD	Audio R RC tune read data
4:0	RGS_AUDRCTUNELREAD	Audio L RC tune read data

2208 **AUDDEC_ANA_CON0** **AUDDEC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRBSCCURRENT_VAUDP15	RG_AUDHPLBSCCURRENT_VAUDP15	RG_AUDHPRSCDISABLE_VAUDP15	RG_AUDHPLSCDISABLE_VAUDP15	RG_AUDHPRMUXINPUTSEL_VAUDP15		RG_AUDHPLMUXINPUTSEL_VAUDP15		RG_AUDHPRPWRUP_IBIAS_VAUDP15	RG_AUDHPLPWRUP_IBIAS_VAUDP15	RG_AUDHPRPWRUP_VAUDP15	RG_AUDHPLPWRUP_VAUDP15	RG_AUD_DAC_PWL_UP_VA28	RG_AUD_DAC_PWR_UP_VA28	RG_AUDDACRPWRUP_VAUDP15	RG_AUDDACLPWRUP_VAUDP15
Type	RW	RW	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDHPRBSCC	**Audio right headphone BSC current**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	URRENT_VAUDP15	
14	RG_AUDHPLBSCCURRENT_VAUDP15	**Audio left headphone BSC current**
13	RG_AUDHPRSCDISABLE_VAUDP15	**Disables headphone right short circuit protection**
12	RG_AUDHPLSCDISABLE_VAUDP15	**Disables headphone left short circuit protection**
11:10	RG_AUDHPRMUXINPUTSEL_VAUDP15	**Selects audio right headphone input multiplexor** Positive/negative pins: 00: Open/Open 01: LOLP/LOLN 10: IDACRP/IDACRN 11: HSP/HSN (test mode)
9:8	RG_AUDHPLMUXINPUTSEL_VAUDP15	**Selects audio left headphone input multiplexor** Positive/negative pins: 00: Open/Open 01: LOLP/LOLN 10: IDACRP/IDACRN 11: HSP/HSN (test mode)
7	RG_AUDHPRPWRUP_IBIAS_VAUDP15	**Powers up audio right headphone bias**
6	RG_AUDHPLPWRUP_IBIAS_VAUDP15	**Powers up audio left headphone bias**
5	RG_AUDHPRPWRUP_VAUDP15	**Powers up audio right headphone**
4	RG_AUDHPLPWRUP_VAUDP15	**Powers up audio left headphone**
3	RG_AUD_DAC_PWL_UP_VA28	**Power down control for left channel audio biasgen** 0: Power down 1: Enable
2	RG_AUD_DAC_PWR_UP_VA28	**Power down control for right channel audio biasgen** 0: Power down 1: Enable
1	RG_AUDDACRPWRUP_VAUDP15	**Power down control for right-channel audio DAC** 0: Power down 1: Enable
0	RG_AUDDACLPWRUP_VAUDP15	**Power down control for left-channel audio DAC** 0: Power down 1: Enable

220A **AUDDEC_ANA_CON1** **AUDDEC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**RG_HPROUTSTGCTRL_VAUDP15**				**RG_HPLOUTSTGCTRL_VAUDP15**			**RG_HPRSHORT2HPRAUX_EN_VA**	**RG_HPLSHORT2HPLAUX_EN_VA**	**RG_HPRAUXFBRSW_EN_VAUDP1**	**RG_HPLAUXFBRSW_EN_VAUDP1**	**RG_AUDHPROUTAUXPWRUP_VAU**	**RG_AUDHPLOUTAUXPWRUP_VA**	**RG_AUDHPROUTPWRUP_VAUDP**	**RG_AUDHPLOUTPWRUP_VAUDP15**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

									UDP 15	UDP 15	5	5	DP15	UDP 15	15	
Type		RW				RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:12	RG_HPROUTSTGCTRL_VAUDP15	**Selects audio right headphone output stage** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x
10:8	RG_HPLOUTSTGCTRL_VAUDP15	**Selects audio left headphone output stage** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x
7	RG_HPRSHORT2HPRAUX_EN_VAUDP15	**Enables audio right headphone main and aux output stages short**
6	RG_HPLSHORT2HPLAUX_EN_VAUDP15	**Enables audio left headphone main and aux output stages short**
5	RG_HPRAUXFBRSW_EN_VAUDP15	**Enables audio right headphone aux feedback resistor for audio depop**
4	RG_HPLAUXFBRSW_EN_VAUDP15	**Enables audio left headphone aux feedback resistor**
3	RG_AUDHPROUTAUXPWRUP_VAUDP15	**Powers up audio right headphone aux output stage**
2	RG_AUDHPLOUTAUXPWRUP_VAUDP15	**Powers up audio left headphone aux output stage**
1	RG_AUDHPROUTPWRUP_VAUDP15	**Powers up audio right headphone main output stage**
0	RG_AUDHPLOUTPWRUP_VAUDP15	**Powers up audio left headphone main output stage**

220C **AUDDEC_ANA_CON2** **AUDDEC Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**RG_HPOUTPUTRESETO_VAUDP1**	**RG_HPINPUTRESET0_VAUDP15**	**RG_HPINPUTSTBENH_VAUDP15**		**RG_HPPSHORT2VCM_VAUDP15**	**RG_AUDREFN_DERES_EN_VAUD**	**RG_AUDHPSTARTUP_VAUDP15**		**RG_HPROUTPUTSTBENH_VAUDP15**				**RG_HPLOUTPUTSTBENH_VAUDP15**		

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

		5					P15									
Type		RW	RW	RW		RW	RW	RW		RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14	RG_HPOUTPUTRESET0_VAUDP15	**HPL/R driver SE output reset to 0V ground** 0: No reset 1: Reset
13	RG_HPINPUTRESET0_VAUDP15	**HP driver input reset to ground** 0: No reset 1: Reset
12	RG_HPINPUTSTBENH_VAUDP15	**HP driver input stability enhancement option** 0: No enhancement 1: Enhance
10	RG_HPPSHORT2VCM_VAUDP15	**HP driver positive output stage short to AU_REFN**
9	RG_AUDREFN_DERES_EN_VAUDP15	**Enables HP ESD resistor @AU_REFN short**
8	RG_AUDHPSTARTUP_VAUDP15	**Forces a Startup mode in HP Amps if required**
6:4	RG_HPROUTPUTSTBENH_VAUDP15	**Enhances HPR output stage STB** [2]: P side Rload, active when [0]=1'b1 0: 250 1: 470 [1]: N side Rload 0: Open 1: 470 [0]: 0: Open 1: Selected by [2] setting
2:0	RG_HPLOUTPUTSTBENH_VAUDP15	**Enhances HPL output stage STB** [2]: P side Rload, active when [0]=1'b1 0: 250 1: 470 [1]: N side Rload 0: Open 1: 470 [0]: 0: Open 1: Selected by [2] setting

220E **AUDDEC_ANA_CON3** **AUDDEC Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_HSOUT_SHORTVCM_VAUDP15**	**RG_HSOUTPUTRESET0_VAUDP15**	**RG_HSINPUTRESET0_VAUDP15**	**RG_HSINPUTSTBENH_VAUDP15**	**RG_HSOUTPUTSTBENH_VAUDP15**	**RG_AUDHSSTARTUP_VAUDP15**	**RG_AUDHSBSCCURRENT_VAUDP15**	**RG_AUDHSSCDISABLE_VAUDP15**	**RG_AUDHSMUXINPUTSEL_VAUDP15**		**RG_AUDHSPWRUP_IBIAS_VAUDP15**	**RG_AUDHSPWRUP_VAUDP15**
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
11	RG_HSOUT_SHORTVCM_VAUDP15	**Short HS output to VCM (DCC: 0V; ACC: 1.4V)** 0: Not short to VCM 1: Short to VCM
10	RG_HSOUTPUTRESET0_VAUDP15	**HS driver DE outputs reset to 0V ground** 0: No reset 1: Reset
9	RG_HSINPUTRESET0_VAUDP15	**HS driver DE inputs reset to 0V ground** 0: No reset 1: Reset
8	RG_HSINPUTSTBENH_VAUDP15	**HS driver input stability enhancement option** 0: No enhancement 1: Enhance
7	RG_HSOUTPUTSTBENH_VAUDP15	**HS driver output stability enhancement option** 0: No enhancement 1: Enhance
6	RG_AUDHSSTARTUP_VAUDP15	**Forces a Startup mode in HS Amp if required**
5	RG_AUDHSBSCCURRENT_VAUDP15	**Audio handset BSC current**
4	RG_AUDHSSCDISABLE_VAUDP15	**Disables headset short circuit protection**
3:2	RG_AUDHSMUXINPUTSEL_VAUDP15	**Selects audio handset input multiplexor** Positive/negative pins: 00: Open/Open 01: Test mode (IDACR) 10: Voice playback 11: Test mode
1	RG_AUDHSPWRUP_IBIAS_VAUDP15	**Powers up audio headset bias**
0	RG_AUDHSPWRUP_VAUDP15	**Powers up audio headset**

2210 **AUDDEC_ANA_CON4** **AUDDEC Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_LOOUT_SHORTVCM_VAUDP15	RG_LOOUTPUTRESET0_VAUDP15	RG_LOINPUTRESET0_VAUDP15	RG_LOOUTPUTSTBENH_VAUDP15	RG_LOINPUTSTBENH_VAUDP15	RG_AUDLOSTARTUP_VAUDP15	RG_AUDLOLBSCCURRENT_VAUDP15	RG_AUDLOLSCDISABLE_VAUDP15	RG_AUDLOLMUXINPUTSEL_VAUDP15		RG_AUDLOLPWRUP_IBIAS_VAUDP15	RG_AUDLOLPWRUP_VAUDP15
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_LOOUT_SHORTVCM_VAUDP15	**Short LO output to VCM (DCC: 0V; ACC: 1.4V)** 0: Not short to VCM 1: Short to VCM

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
10	RG_LOOUTPUTRESET0_VAUDP15	**LOL/R driver SE output reset to 0V ground** 0: No reset 1: Reset
9	RG_LOINPUTRESET0_VAUDP15	**LO driver input reset to ground** 0: No reset 1: Reset
8	RG_LOOUTPUTSTBENH_VAUDP15	**LO driver output stability enhancement option** 0: No enhancement 1: Enhance
7	RG_LOINPUTSTBENH_VAUDP15	**LO driver input stability enhancement option** 0: No enhancement 1: Enhance
6	RG_AUDLOSTARTUP_VAUDP15	**Forces a Startup mode in LO Amps if required**
5	RG_AUDLOLBSCCURRENT_VAUDP15	**Audio left LO buffer BSC current**
4	RG_AUDLOLSCDISABLE_VAUDP15	**Disables LO buffer left short circuit protection**
3:2	RG_AUDLOLMUXINPUTSEL_VAUDP15	**Selects audio left LO buffer input multiplexor** Positive/negative pins: 00: Open/Open 01: Test mode (IDACR) 10: Audio playback 11: Test mode
1	RG_AUDLOLPWRUP_IBIAS_VAUDP15	**Powers up audio left LO buffer bias**
0	RG_AUDLOLPWRUP_VAUDP15	**Powers up audio left LO buffer**

2212 **AUDDEC_ANA_CON5** **AUDDEC Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_AUDHPSPKDET_EN_VAUDP15	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15		RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15			RG_AUDTRIMBUF_EN_VAUDP15	RG_AUDTRIMBUF_GAINSEL_VAUDP15		RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15			
Type				RW	RW		RW			RW	RW		RW			
Reset				0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
12	RG_AUDHPSPKDET_EN_VAUDP15	**Enables audio headphone speaker detection**
11:10	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15	**Selects audio headphone speaker detection output mux** 00: Open 01: HPL 10: HPR 11: Unused
9:8	RG_AUDHPSPKDE	**Enables audio headphone speaker detection input mux**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	T_INPUTMUXSEL_VAUDP15	00: Open 01: DACLP 10: DACLN 11: DACRP
6	RG_AUDTRIMBUF_EN_VAUDP15	**Enables audio offset trimming buffer**
5:4	RG_AUDTRIMBUF_GAINSEL_VAUDP15	**Selects audio offset trimming buffer gain** 00: 0dB 01: 6dB 10: 12dB 11: 18dB
3:0	RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15	**Selects audio offset trimming buffer mux** 0000: Open 0001: HPL 0010: HPR 0011: HSP 0100: HSN 0101: LOLP 0110: LOLN 0111: LORP 1000: LORN 1001: AVSS32 1010~1111: Unused

2214 **AUDDEC_ANA_CON6** **AUDDEC Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD0_VAUDP15								RG_ABIDEC_RSVD0_VA28							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD0_VAUDP15	**Reserved one byte in VAUDP15 domain** [7:4]: HP Aux loop gain setting [3]: Enable HPR aux CMFB loop [2]: Enable HPL aux CMFB loop [1]: Enable HPR/L main CMFB loop [0]: Enable HP output stage turn on timing control
7:0	RG_ABIDEC_RSVD0_VA28	**Reserved one byte in VA28 domain** [0]: Low-noise mode of DAC enable 1'b0: Disable 1'b1: Enable [1]: Enable trim buffer 1'b0: Disable 1'b1: Enable [7]: HP CMFB rstb 1'b0: Reset 1'b1: Normal operation

2216 **AUDDEC_ANA_CON7** **AUDDEC Control Register 7** **0000**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD2_VAUDP15								RG_ABIDEC_RSVD1_VAUDP15							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD2_VAUDP15	Reserved one byte in VAUDP15 domain
7:0	RG_ABIDEC_RSVD1_VAUDP15	Reserved one byte in VAUDP15 domain

2218 **AUDDEC_ANA_CON8** **AUDDEC Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_AUDZCDCLKSEL_VAUDP15	RG_AUDZCDMUXSEL_VAUDP15		
Type													RW	RW		
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_AUDZCDCLKSEL_VAUDP15	**Increases ZCD comparator speed** 0: Normal speed 1: Improved speed
2:0	RG_AUDZCDMUXSEL_VAUDP15	**Selects zero crossing detection mux** 000: LOL 001: HPL and HPR 010: Handset 011: Unused 100: Bypass ZCD

221A **AUDDEC_ANA_CON9** **AUDDEC Control Register 9** **0092**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_AUDBIASADJ_0_VAUDP15								
Type								RW								
Reset								0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
8:0	RG_AUDBIASADJ_0_VAUDP15	**Audio bias adjustment 0, bits:** [2:0] Headphone left/right DR bias current setting: [5:3] Handset DR bias current setting. DR bias settings: [8:6] Line-out DR bias current setting. DR bias settings: 000: 4uA 001: 5uA 010: 6uA 011: 7uA

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		100: 8uA 101: 9A 110: 10uA 111: 11uA

221C **AUDDEC_ANA_CON10** **AUDDEC Control Register 10** **0155**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_AUDIBIASPWRDN_VAUDP15	RG_AUDBIASADJ_1_VAUDP15							
Type								RW	RW							
Reset								1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
8	RG_AUDIBIASPWRDN_VAUDP15	**Power down control for IbiasDistrib circuit** 0: Enable 1: Disable
7:0	RG_AUDBIASADJ_1_VAUDP15	**Audio bias adjustment 1, bits:** [7:6] ZCD bias current setting 00: 3uA 01: 4uA 10: 5uA 11: 6uA [5:4] LOL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [3:2] HS ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [1:0]: HPL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA

221E **AUDDEC_ANA_CON11** **AUDDEC Control Register 11** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_SEL_ENCODER_96K	RG_RSTB_ENCODER_VA	RG_AUDGLB_PWRDN_VA		RG_SEL_DELAY_VCORE	RG_SEL_DECODER_96K	RG_RSTB_DECODER_VA

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

										_VA28	28	28			_VA28	28
Type										RW	RW	RW		RW	RW	RW
Reset										0	0	1		0	0	0

Bit(s)	Name	Description
6	RG_SEL_ENCODER_96K_VA28	**Selects audio ADC clock** 0: 3.25MHz 1: 6.5MHz
5	RG_RSTB_ENCODER_VA28	**Resets audio encoder** 0: Reset 1: Normal
4	RG_AUDGLB_PWRDN_VA28	**Power down control for audio global bias circuit** 0: Enable 1: Disable; default on
2	RG_SEL_DELAY_VCORE	**Selects AFIFO read clock delay** 0: 5ns 1: 10ns
1	RG_SEL_DECODER_96K_VA28	**Selects audio DAC clock** 0: 3.25MHz 1: 6.5MHz
0	RG_RSTB_DECODER_VA28	**Resets audio decoder** 0: Reset 1: Normal

2220 **AUDDEC_ANA_CON12** **AUDDEC Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VA28REFGEN_EN_VA28	RG_VA33REFGEN_EN_VA18		RG_LCLDO_ENC_REMOTE_SENSE_VA28	RG_LCLDO_ENC_PDDIS_EN_VA28	RG_LCLDO_ENC_EN_VA28		RG_LCLDO_REMOTE_SENSE_VA18	RG_LCLDO_PDDIS_EN_VA18	RG_LCLDO_EN_VA18		RG_HCLDO_REMOTE_SENSE_VA18	RG_HCLDO_PDDIS_EN_VA18	RG_HCLDO_EN_VA18
Type			RW	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW
Reset			0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
13	RG_VA28REFGEN_EN_VA28	**Enables LCLDO_ENC Ref. gen.**
12	RG_VA33REFGEN_EN_VA18	**Enables HC_LDO, LC_LDO Ref. gen.**
10	RG_LCLDO_ENC_REMOTE_SENSE_VA28	**Selects LCLDO_ENC remote sense function** 0: Local sense 1: Remote sense
9	RG_LCLDO_ENC_PDDIS_EN_VA28	**Enables LCLDO_ENC power down discharge**
8	RG_LCLDO_ENC_EN_VA28	**Enables LCLDO_ENC**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
6	RG_LCLDO_REMOTE_SENSE_VA18	**Selects LCLDO remote sense function** 0: Local sense 1: Remote sense
5	RG_LCLDO_PDDIS_EN_VA18	**Enables LCLDO power down discharge**
4	RG_LCLDO_EN_VA18	**Enables LCLDO**
2	RG_HCLDO_REMOTE_SENSE_VA18	**Selects HCLDO remote sense function** 0: Local sense 1: Remote sense
1	RG_HCLDO_PDDIS_EN_VA18	**Enables HCLDO power down discharge**
0	RG_HCLDO_EN_VA18	**Enables HCLDO**

2222 **AUDDEC_ANA_CON13** **AUDDEC Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_AUDPMU_RSD0_VA18						RG_NVREG_PULL0V_VAUDP15	RG_NVREG_EN_VAUDP15
Type									RW						RW	RW
Reset									0	0	0	0			0	0

Bit(s)	Name	Description
7:4	RG_AUDPMU_RSD0_VA18	**Reserved in VA18/GND domain**
1	RG_NVREG_PULL0V_VAUDP15	0: DCC mode, switch is opened, NV output is -0.95V. 1: ACC mode, switch is closed, NV reg output is pulled to GND.
0	RG_NVREG_EN_VAUDP15	**Enables NVREG**

2226 **AUDDEC_ELR_0** **AUDDEC ELR 0 register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_AUDHPTRIM_EN_VAUDP15	RG_AUDHPRFINETRIM_VAUDP15		RG_AUDHPLFINETRIM_VAUDP15		RG_AUDHPRTRIM_VAUDP15				RG_AUDHPLTRIM_VAUDP15			
Type				RW	RW		RW		RW				RW			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
12	RG_AUDHPTRIM_EN_VAUDP15	**Enable control of trim circuit of HP. (0): disable trim circuit (1): enable trim circuit**
11:10	RG_AUDHPRFINETRIM_VAUDP15	**Fine-trims offset voltage of HPR** 01: -0.5mV 10: +0.5mV
9:8	RG_AUDHPLFINETRIM_VAUDP15	**Fine-trims offset voltage of HPL** 01: -0.5mV 10: +0.5mV
7:4	RG_AUDHPRTRIM_VAUDP15	**Trims offset voltage of HPR** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
3:0	RG_AUDHPLTRIM_VAUDP15	**Trims offset voltage of HPL** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV

2288 ZCD_CON0 ZCD Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDZCDTIMEOUTMODESEL	RG_AUDZCDGAINSTEPSIZE		RG_AUDZCDGAINSTEPTIME			RG_AUDZCDENABLE
Type										RW	RW		RW			RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	RG_AUDZCDTIME	**If no zero crossings are detected over a period of 30ms/5ms, a**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	OUTMODESEL	**timeout will occur and the ZCD block enter SILENT mode.** 0: 30ms 1: 5ms
5:4	RG_AUDZCDGAIN STEPSIZE	**Gain Step size to change the internal gain of ZCD.** 00: 1dB. 01: 2dB. 10: 4dB. 11: 8dB.
3:1	RG_AUDZCDGAIN STEPTIME	**Gain Step Time to change the internal gain of ZCD.** 000: 0 us. 001: 250 us 010: 500 us. 011: 1 ms. 100: 2 ms. 101: 4 ms. 110: 8 ms. 111: 16 ms.
0	RG_AUDZCDENAB LE	**Enable for zero crossing detection (ZCD) function.** 0: Disable 1: Enable

228A ZCD_CON1 ZCD Control Register 1 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDLORGAIN							RG_AUDLOLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDLORGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDLOLGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB (mute)

228C ZCD_CON2 ZCD Control Register 2 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPRGAIN							RG_AUDHPLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDHPRGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDHPLGAIN	00000: +8dB. 00001: +7dB.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		10010: -10dB 11111: -40dB (mute)

228E ZCD_CON3 ZCD Control Register 3 001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_AUDHSGAIN				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	RG_AUDHSGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB (mute)

2290 ZCD_CON4 ZCD Control Register 4 0707

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDIVRGAIN								RG_AUDIVLGAIN		
Type						RW								RW		
Reset						1	1	1						1	1	1

Bit(s)	Name	Description
10:8	RG_AUDIVRGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB
2:0	RG_AUDIVLGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB

2292 ZCD_CON5 ZCD Control Register 5 3F3F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDINTGAIN2								RG_AUDINTGAIN1					
Type			RO								RO					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
13:8	RG_AUDINTGAIN2	Monitor signal: internal gain2

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
5:0	RG_AUDINTGAIN1	Monitor signal: internal gain1

2308 ACCDET_CON0 ACCDET Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUDACCDETAUXADCSWCTRL_SEL											
Type					RW											
Reset					0											

Bit(s)	Name	Description
11	AUDACCDETAUXADCSWCTRL_SEL	**Controls the DA_NI_AUDACCDETAUXADCSWTROL signal is from SW or HW** 1'b0: HW mode 1'b1: SW mode

230A ACCDET_CON1 ACCDET Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ACCDET_ANASWCTRL_SEL	ACCDET_EINT1_SEQ_INIT	ACCDET_EINT1_EN	ACCDET_EINT0_SEQ_INIT	ACCDET_EINT0_EN	ACCDET_SEQ_INIT	ACCDET_EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	ACCDET_ANASWCTRL_SEL	**Selects who controls the connection between AUXADC and ACCDET when in hook-key status** 1'b0: AUXADC 1'b1: ACCDET
5	ACCDET_EINT1_SEQ_INIT	**Initializes EINT1 status default value** 1'b0: Disable 1'b1: Enable
4	ACCDET_EINT1_EN	**Enables EINT1 detection** 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT0_SEQ_INIT	**Initializes EINT0 status default value** 1'b0: Disable 1'b1: Enable
2	ACCDET_EINT0_E	**Enables EINT0 detection**

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
	N	1'b0: Disable 1'b1: Enable
1	ACCDET_SEQ_INIT	**Initializes ACCDET status default value** 1'b0: Normal mode 1'b1: Initialized mode
0	ACCDET_EN	**Enables ACCDET** Must be set to 0 before switching to TV mode 1'b0: Disable 1'b1: Enable

230C **ACCDET_CON2** **ACCDET Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ACCDET_EINT1_PWM_EN	ACCDET_EINT0_PWM_EN	ACCDET_MBIAS_PWM_EN	ACCDET_VTH_PWM_EN	ACCDET_CMP_PWM_EN
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	ACCDET_EINT1_PWM_EN	**Enables PWM of ACCDET EINT1 unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT0_PWM_EN	**Enables PWM of ACCDET EINT0 unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
2	ACCDET_MBIAS_PWM_EN	**Enables PWM of ACCDET MBIAS unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
1	ACCDET_VTH_PWM_EN	**Enables PWM of ACCDET voltage threshold unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
0	ACCDET_CMP_PWM_EN	**Enables PWM of ACCDET comparator** 1'b0: Disable 1'b1: Enable

230E **ACCDET_CON3** **ACCDET Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:0	ACCDET_PWM_WIDTH	**ACCDET PWM width** PWM output frequency = 32,768/(PWM_WIDTH + 1)Hz

2310 **ACCDET_CON4** **ACCDET Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_THRESH	**ACCDET PWM threshold** PWM output duty cycle = (PWM_THRESH + 1)/(PWM_WIDTH + 1) PWM output high time = (PWM_THRESH + 1)/32,768 sec

2312 **ACCDET_CON5** **ACCDET Control Register 5** **0101**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_FALL_DELAY	ACCDET_RISE_DELAY														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	ACCDET_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET is disabled, the suitable falling delay cycle is necessary.
14:0	ACCDET_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET is enabled, the suitable rising delay cycle is necessary.

2314 **ACCDET_CON6** **ACCDET Control Register 6** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE0	**De-bounce time control of state 0** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768 Hz in the MIC mode.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

2316 ACCDET_CON7 ACCDET Control Register 7 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE1	**De-bounce time control of state 1** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768 Hz in the MIC mode.

2318 ACCDET_CON8 ACCDET Control Register 8 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE2	**De-bounce time control of state 2** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768 Hz in the MIC mode.

231A ACCDET_CON9 ACCDET Control Register 9 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE3	**De-bounce time control of state 3** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768 Hz in the MIC mode.

231C ACCDET_CON10 ACCDET Control Register 10 0005

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE4	De-bounce time to control AUXADC when in state 0

2320 **ACCDET_CON12** **ACCDET Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT1_IRQ_POLARITY	ACCDET_EINT0_IRQ_POLARITY			ACCDET_EINT1_IRQ_CLR	ACCDET_EINT0_IRQ_CLR		ACCDET_IRQ_CLR					ACCDET_EINT1_IRQ	ACCDET_EINT0_IRQ		ACCDET_IRQ
Type	RW	RW			RW	RW		RW					RO	RO		RO
Reset	0	0			0	0		0					0	0		0

Bit(s)	Name	Description
15	ACCDET_EINT1_IRQ_POLARITY	**ACCDET EINT1 IRQ POLARITY** 1'b0: Falling edge 1'b1: Rising edge
14	ACCDET_EINT0_IRQ_POLARITY	**ACCDET EINT0 IRQ POLARITY** 1'b0: falling edge 1'b1: rising edge
11	ACCDET_EINT1_IRQ_CLR	**Clears ACCDET_EINT1 interrupt status** When ACCDET_EINT1 interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT1 design until both the interrupt status and IRQ_CLR are cleared.
10	ACCDET_EINT0_IRQ_CLR	**Clears ACCDET_EINT0 interrupt status** When ACCDET_EINT0 interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.
8	ACCDET_IRQ_CLR	**Clears ACCDET interrupt status** When ACCDET interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET design until both the interrupt status and IRQ_CLR are cleared.
3	ACCDET_EINT1_IRQ	**Clears ACCDET_EINT1 interrupt status**
2	ACCDET_EINT0_IRQ	**Clears ACCDET_EINT0 interrupt status**
0	ACCDET_IRQ	**ACCDET interrupt status** Due to this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design.

2324 **ACCDET_CON14** **ACCDET Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_AUDACC	ACCDET_CM	ACCDET_VT	ACCDET_MB												

© 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

	DET AUX ADC SWC TRL	P_C LK	H_C LK	IAS_ CLK												
Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	DA_AUDACCDETAUXADCSWCTRL	ACCDET to AUXADC switch control
14	ACCDET_CMP_CLK	Comparator turn on control for accessory detection
13	ACCDET_VTH_CLK	Threshold voltage turn on for accessory detection
12	ACCDET_MBIAS_CLK	Earphone bias voltage turn on for accessory detection

2326 **ACCDET_CON15** **ACCDET Control Register 15** **0071**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT0_PWM_WIDTH			ACCDET_EINT0_PWM_THRESH				ACCDET_EINT0_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	1	0			

Bit(s)	Name	Description
13:12	ACCDET_EINT0_PWM_WIDTH	**ACCDET EINT0 PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT0_PWM_THRESH	**ACCDET EINT0 PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:3	ACCDET_EINT0_DEBOUNCE	**ACCDET EINT0 debounce time** 4'd0: 0ms (bypass) 4'd1: 0.12ms 4'd2: 0.25ms 4'd3: 0.5ms 4'd4: 0.75ms 4'd5: 1ms 4'd6: 2ms 4'd7: 4ms 4'd8: 8ms 4'd9: 16ms 4'd10: 32ms 4'd11: 48ms 4'd12: 64ms 4'd13: 128ms

© 2017 MediaTek Inc.
This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Bit(s)	Name	Description
		4'd14: 256ms 4'd15: 512ms

2328 **ACCDET_CON16** **ACCDET Control Register 16** **0160**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT0_PWM_RISE_DELAY										ACCDET_EINT0_PWM_FALL_DELAY					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	1	0	1	1					

Bit(s)	Name	Description
15:6	ACCDET_EINT0_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT0_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT is disabled, the suitable falling delay cycle is necessary.

232C **ACCDET_CON18** **ACCDET Control Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_EINT0CMPEN	AD_EINT0CMPOUT														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_NI_EINT0CMPEN	Monitor signal: DA_NI_EINT0CMPEN
14	AD_EINT0CMPOUT	Monitor signal: AD_EINT0CMPOUT

2332 **ACCDET_CON21** **ACCDET Control Register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ACCDET_MON_FLAG_SEL											ACCDET

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

																_MON_FLAG_EN
Type					RW											RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:4	ACCDET_MON_FLAG_SEL	Selects accdet monitor flag
0	ACCDET_MON_FLAG_EN	Enables accdet monitor flag

233A ACCDET_CON25 ACCDET Control Register 25 0071

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT1_PWM_WIDTH			ACCDET_EINT1_PWM_THRESH				ACCDET_EINT1_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	1	0			

Bit(s)	Name	Description
13:12	ACCDET_EINT1_PWM_WIDTH	**ACCDET EINT1 PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT1_PWM_THRESH	**ACCDET EINT1 PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:3	ACCDET_EINT1_DEBOUNCE	**ACCDET EINT1 debounce time** 4'd0: 0ms (bypass) 4'd1: 0.12ms 4'd2: 0.25ms 4'd3: 0.5ms 4'd4: 0.75ms 4'd5: 1ms 4'd6: 2ms 4'd7: 4ms 4'd8: 8ms 4'd9: 16ms 4'd10: 32ms 4'd11: 48ms 4'd12: 64ms 4'd13: 128ms 4'd14: 256ms 4'd15: 512ms

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

233C **ACCDET_CON26** **ACCDET Control Register 26** **0160**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT1_PWM_RISE_DELAY										ACCDET_EINT1_PWM_FALL_DELAY					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	1	0	1	1					

Bit(s)	Name	Description
15:6	ACCDET_EINT1_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT1 is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT1_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT1 is disabled, the suitable falling delay cycle is necessary.

233E **ACCDET_CON27** **ACCDET Control Register 27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_EINT1CMPEN	AD_EINT1CMPOUT														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_NI_EINT1CMPEN	Monitor signal: DA_NI_EINT1CMPEN
14	AD_EINT1CMPOUT	Monitor signal: AD_EINT1CMPOUT

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

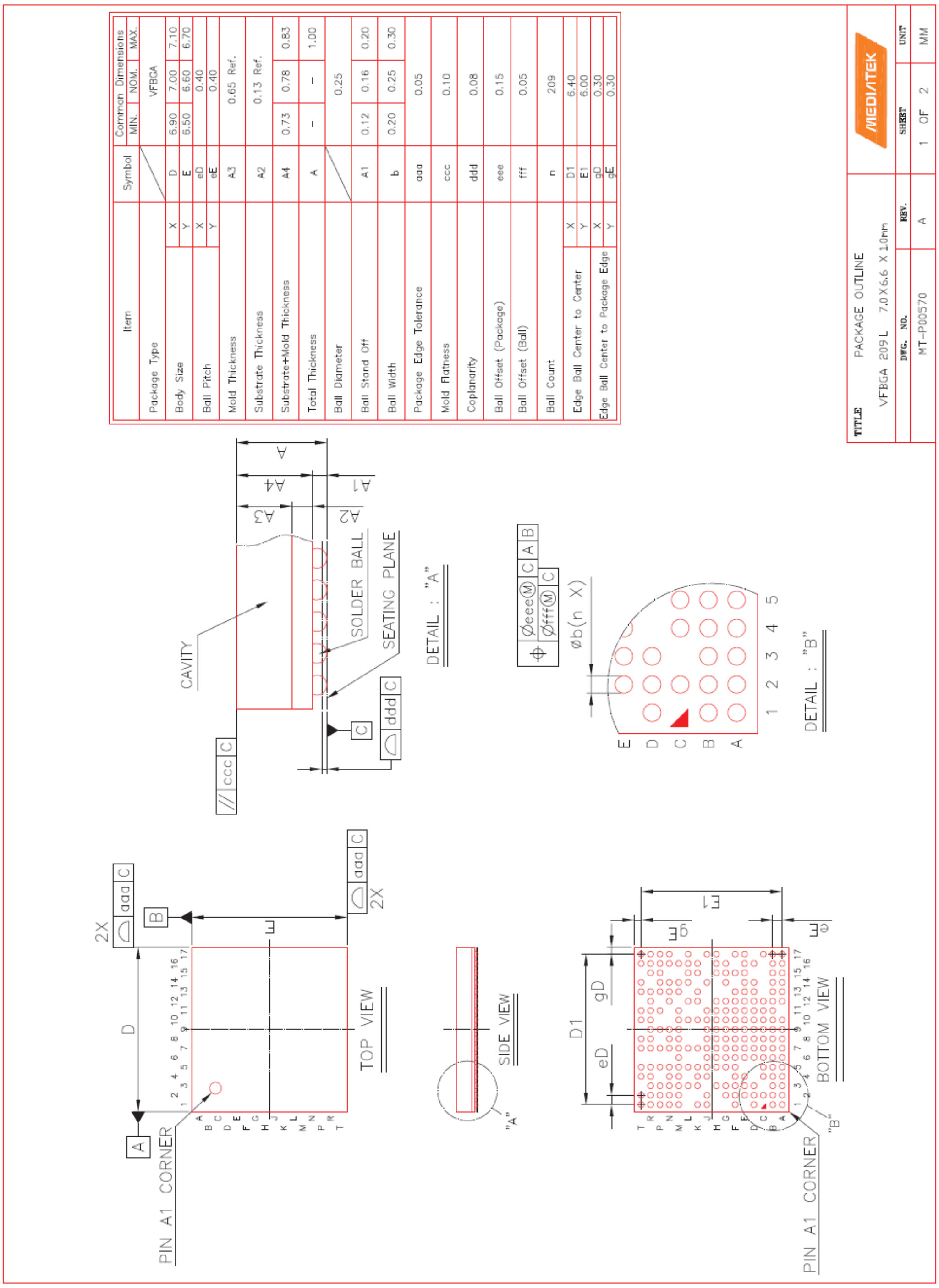
4 Application Notes

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

5 MT6357 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	6.90	7.00	7.10
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.13 Ref.	
Substrate+Mold Thickness		A4	0.73	0.78	0.83
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		209	
Edge Ball Center to Center	X	D1		6.40	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 5-1. Package dimension

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.

Appendix

© 2017 MediaTek Inc.

This document contains information that is proprietary to MediaTek Inc.
Unauthorized reproduction or disclosure of this information in whole or in part is strictly prohibited.